ISSN:2348-2079

Volume-7 Issue-1

International Journal of Intellectual Advancements and Research in Engineering Computations

Dual-quality 5:2 compressors for utilizing in dynamic accuracy configurable multipliers

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ABSTRACT

The dual-quality reconfigurable approximate 5:2 compressor has the ability to switching between the exact and approximate operating modes during the runtime. It utilizes architecture of dynamic quality configurable parallel multipliers. The basic structure of the compressor consists two parts such as approximate mode and exact mode. In the approximate mode, dual-quality compressors having high speed and low power consumption at the cost of lower accuracy. The number of gates and delay has reduced by using 5:2 compressors. Each of these compressors has its own level of accuracy, delay and power dissipations in both approximate and exact modes. The efficiencies of these compressors in a 32-bit Dadda multiplier are evaluated in a 45nm standard CMOS technology by comparing their parameters with approximate multipliers. The developed 5:2 compressors used in more realization of multi-operand addition and partial product reduction. It gives an average of 46% lower delay and68% power consumption in the approximate mode. The effectiveness of these compressors is assessed in some image processing applications like image segmentation and image multiplication.

INTRODUCTION

In recent years, power consumption has become a critical design concern for many VLSI systems. It is an important parameter in portable battery-operated applications where the power consumption may be more important than speed and area. The multiplier is one of the main blocks, which is widely used in different applications digital signal processing applications. There are two general architectures for the multipliers, which are sequential and parallel. While sequential architectures are low power latency is very large. On the other hand, parallel architectures (such as Wallace tree and Dadda) are fast while having high-power consumptions. The parallel multipliers are used in high-performance applications where their large power consumptions may create hot-spot locations on the die. Since the power consumption and speed are critical parameters in the design of digital circuit, approximate computing approaches are based on achieving the target specifications at the cost of reducing the computation accuracy. These applications include multimedia processing, machine learning, signal processing, and other error resilient computations.

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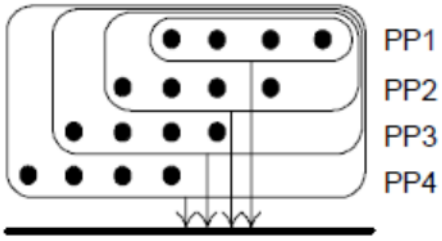


Figure 1.1Multiplier

Approximate arithmetic units are mainly based on the simplification of the arithmetic units circuits. There are many prior works focusing on approximate multipliers. In what follows, the terms multiplicand and multiplier refer to the first and second operands of a given multiplication, respectively. In each multiplication step, one or more multiples of the multiplicand are generated and added to the partial sum through a two- or multi-operand addition operation. To reduce the power consumption of the multiplier and clock tick count required for the completion of a multiplication can lower the power consumption of the flipflops and increase the speed of the circuit. This will reduce the power delay product (PDP) factor of the circuit.

OVERVIEW OF MULTIPLIER

Multiplication is a fundamental operation in most signal processing algorithms. Multipliers have large area, long latency and consume considerable power. Therefore low power multiplier design has an important part in low-power VLSI system design. A system is generally determined by the performance of the multiplier because the multiplier is generally the slowest element and more area consuming in the system. Hence optimizing the speed and area of the multiplier is one of the major design issues. However, area and speed are usually conflicting constraints so that improvements in speed results in larger areas. Multiplication is a mathematical operation that include process of adding an integer to itself a specified number of times. A number (multiplicand) is added itself a number of times as specified by another number (multiplier) to form a result (product). Multipliers play an important role in today's digital signal processing and various other applications. Multiplier design should offer high speed, low power consumption.

Multiplication involves mainly 3 steps

- Partial product generation
- Partial product reduction
- Final addition

Compressor

The 4-2 compressor is another widely used building block for high precision and high speed multipliers. The block diagram of the 4:2 compressor is shown in the figure, which has four inputs and three outputs. In 4:2 compressor block, four of the inputs are the primary inputs X0, X1, X2 and X3 and the output sum has some weight. In is the output carry of preceding module and Cout, the carry output of this stage is fed to the next compressor. The output carry is weighted one binary bit order higher.

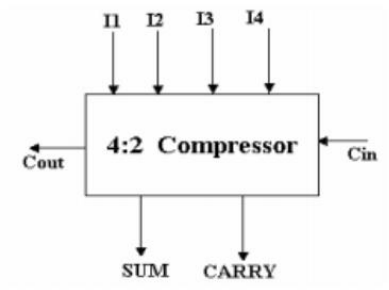


Figure 1.4 4:2 Compressor

The compressor is governed by following basic equation:

X1+X2+X3+X4+Cin= Sum+2*(Carry+ Cout).

LITERATURE SURVEY

Chip-Hong Chang (2004), described a several architectures and designs of low-power 4-2 and 5-2 compressors capable of operating at ultra-low supply voltages. These compressor architectures are anatomized into their constituent modules and different static logic styles based on the same deep sub-micrometer CMOS process model are used to realize them. Different configurations of each architecture, which include a number of novel 4-2 and 5-2 compressor designs, are prototyped and simulated to evaluate their performance in speed, power dissipation and power-delay product. The proposed new circuit for the XOR–XNOR module eliminates the weak logic on the internal nodes of pass transistors with a pair of feedback PMOS–NMOS transistors. Driving capability has been considered in the design as well as in the simulation setup so that these 4-2 and 5-2 compressor cells can operate reliably in any tree structured parallel multiplier at very low supply voltages.

Cong Liu, et al (2014), [2] Approximate circuits have been considered for error-tolerant applications that can tolerate some loss of accuracy with improved performance of energy efficiency. Multipliers are arithmetic circuits in many such applications digital signal processing (DSP).A novel approximate multipliers with lower power consumption and a shorter critical path than traditional multiplier is proposed for high performance accuracy as traditional exact multipliers but with significant Improvements in power and performance.

Gao,et al (2007), [5] presents an optimized design approach of two's compliment large size multipliers using embedded multipliers in FPGAs. The realization is based on baugh-wooley's algorithm. To achieve efficient implementation, a set of optimized schemes for the addition of partial is proposed. The implementations of the multipliers are carried out for operands with sizes from 20 to 128 bits. The results indicate that the proposed approach outperforms the traditional methods by 50% in terms of LUT-delay product.

Lucas, et al (2010), [6] described the conventional digital hardware computational blocks with different structures are designed to compute the precise results of the assigned calculations. The main contribution of our proposed Bio-inspired Imprecise Computational blocks (BICs) is that they are designed to provide an applicable estimation of the result instead of its precise value at a lower cost. These novel structures are more efficient in terms of area, speed, and power consumption with respect to their precise rivals. Complete descriptions of sample BIC adder and multiplier structures as well as their error behaviors and synthesis results are introduced in this paper. It is then shown that these BIC structures can be exploited to efficiently implement a three-layer face recognition neural network and the hardware defuzzification block of a fuzzy processor.

Khaing Yin Kyaw, et al (2010), [7] described the new design concept that engaged accuracy as a design parameter is proposed. By introducing accuracy as a design parameter, the bottleneck of conventional digital IC design techniques can be breakthrough to improve on the performances of power consumption and speed. The aim is to fulfill the need for high performance basic sequential elements with low-power dissipation which is steadily growing.

Srinivasan Narayanamoorthy, et al (2010), described the need to support various digital signal processing (DSP) and classification applications on energy constrained devices in a regular manner. Such applications often extensively perform matrix multiplications using fixed-point arithmetic while exhibiting tolerance for some computational errors. Hence, improving the energy efficiency of multiplications is critical. Architecture of multipliers can trade-off computational accuracy with energy consumption at design time. Compared with a precise multiplier, the proposed multiplier can consume 58% less energy/op with average computational error of ~1%. Demonstrate that such a small computational error does not notably impact the quality of DSP and the accuracy of classification applications.

PROPOSED METHODOLOGY

Exact 4:2 compressor

To reduce the delay of the partial product summation stage of parallel multipliers, 4:2 and 5:2 compressors are widely employed. Some compressor in the structure has been optimized for one or more design parameters such as delay, area, and power consumption. First, some background on the exact 4:2 compressor is presented. This type of compressor, shown schematically in Fig.3.1, has four inputs ($x1$–$x4$) along with an input carry (Cin), and two outputs (sumand carry) along with an output $Cout$. The internal structure of an exact 4:2 compressor is composed of two serially connected full adders, as shown in Fig. 2.In this structure, the weights of all the inputs and the sum output are the same whereas the weights of the carry and $Cout$ outputs are one binary bit position higher. The outputs sum, carry, and $Cout$ are obtained from.

$$\text{sum} = x1 \oplus x2 \oplus x3 \oplus x4 \oplus Cin$$

$$\text{carry} = (x1 \oplus x2 \oplus x3 \oplus x4)Cin + \overline{(x1 \oplus x2 \oplus x3 \oplus x4)}x4$$

$$\text{Cout} = (x1 \oplus x2)x3 + \overline{(x1 \oplus x2)}x1.$$

The proposed DQ4:2Cs operate in two accuracy modes of approximate and exact. The diagram consists of two main parts of approximate and supplementary. During the approximate mode, only the approximate part is exploited while the supplementary part is power gated. During the exact operating mode, the supplementary and some parts of the approximate parts are utilized.

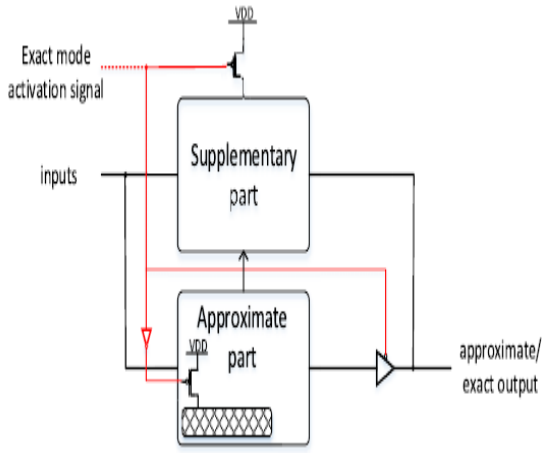


Figure Block diagram of the proposed approximate 4:2 compressors

By reducing the power consumption and area, most of the components of the approximate part are also used during the exact operating mode. We use the power gating technique to turn OFF the unused components of the approximate part. Also note that, in the exact operating mode, tri state buffers are utilized to disconnect the outputs of the approximate part from the primary outputs. In this design, the switching between the approximate and exact operating modes is fast. Thus, it provides us with the opportunity of designing parallel multipliers that are capable of switching between different accuracy levels during the runtime. Next, we discuss the details of our four DQ4:2Cs based on the diagram. The structures have different accuracies, delays, power consumptions, and area usages. Note that the i^{th}proposed structure is denoted by DQ4:2C*i*. The basic idea behind suggesting the approximate compressors was to minimize the difference (error) between the outputs of exact and approximate ones. Therefore, in order to choose the proper approximate designs

for the compressors, an extensive search was performed.

DESCRIPTION

Compressor

5:2 compressor having five inputs X1, X2, X3, X4, X5 and two carry inputs Cin1 and Cin2 and produces 4 outputs like Sum, Carry, Cout1 and Cout2.

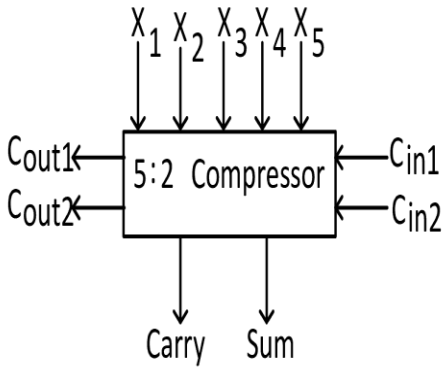


Figure 3.2 5:2 Compressor

5:2 compressor having five inputs X1, X2, X3, X4, X5 and two carry inputs Cin1 and Cin2 and produces 4 outputs like Sum, Carry, Cout1 and Cout2. The input carry bits are the outputs from the previous block of compressor and the output carries are given to the successive stage of compressor. This can be implemented by using three stages of full adders which are connected in series. A faster 5:2 compressor is proposed to architecture different method to generate a cout1 and the proposed multiplier uses in the first part, the AND gates to generate all partial products. An 8×8 unsigned Dadda tree multiplier is considered to access the impact of using the proposed compressors in approximate multipliers.

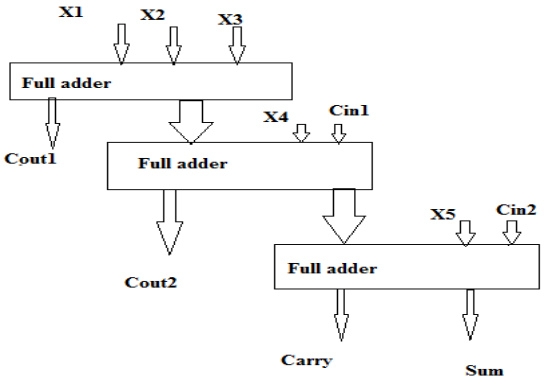


Figure Full Adder using 5:2 Compressor

DADDA MULTIPLIER USING 5:2 COMPRESSOR

Dadda multipliers are refinement of parallel multipliers and offered by Wallace in 1964. The maximum height of each phase is predicted from final stage which contains two rows of partial products. Partial product acquired after multiplication was obtained at the first stage.

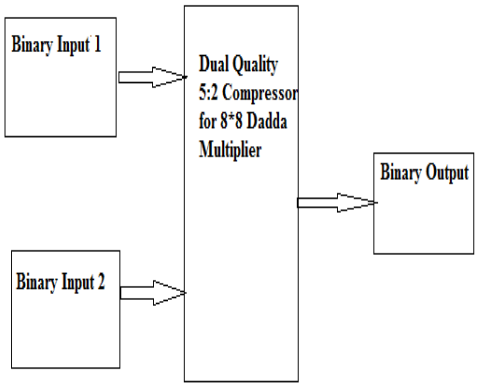


Figure Dual Quality for 5:2 Compressor

The data's are obtained with 3 wires and added using 5:2 compressors and then the carry of each stage was added with next two data in the same stage. Partial products reduced to two layers using compressors with same procedure. At the final stage, 5:2 compressor techniques are used to perform the product operation. Schematic diagram of Dadda multiplier with modified 5:2 compressors.

Proposed dual quality compressor

Dadda multipliers are refinement of parallel multipliers and offered by Wallace in 1964. The maximum height of each phase is predicted from final stage which contains two rows of partial products. Reduction phase in modified Dadda multiplier with 5:2 compressor techniques are shown in Figure 3.6.

Steps involved in DADDA multipliers with 5:2 compressor techniques:

- Multiply (AND operation) each bit by each bit of other arguments, obtaining N results.
- Reduce the total number of partial products to 4 stages.
- Normal Dadda multiplier uses conventional adder (half adder, full adder and carry look ahead adder) but Dadda multiplier with compressor reduces the summation steps and state transition steps, delay and power consumption.

The partial product acquired after multiplication was obtained at the first stage. The data are obtained with 3 wires and added using 5:2 compressors and then the carry of each stage was added with next two data in the same stage. Partial products reduced to two layers using compressors with same procedure. At the final stage, 5:2 compressor techniques are used to perform the product operation.

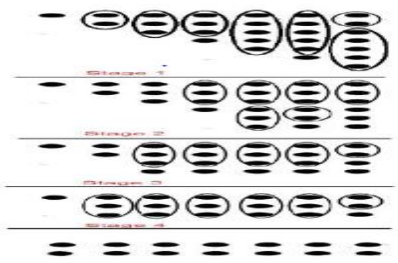


Figure Reduction phase in modified Dadda multiplier with 5:2 compressor techniques

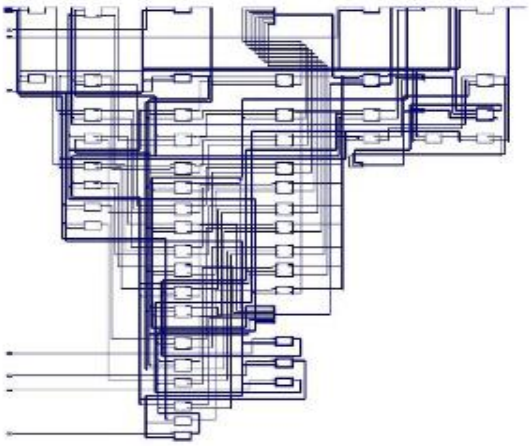


Figure Schematic diagram of Dadda multiplier with modified 5:2 compressors

RESULTS AND DISCUSSION

Simulation results

Figure 4.1shows the approximate multiplier using Dual Quality for 5:2 compressors. Here initially clock signal is set as 1 and inputis 11111100and it produces output as 00011111.

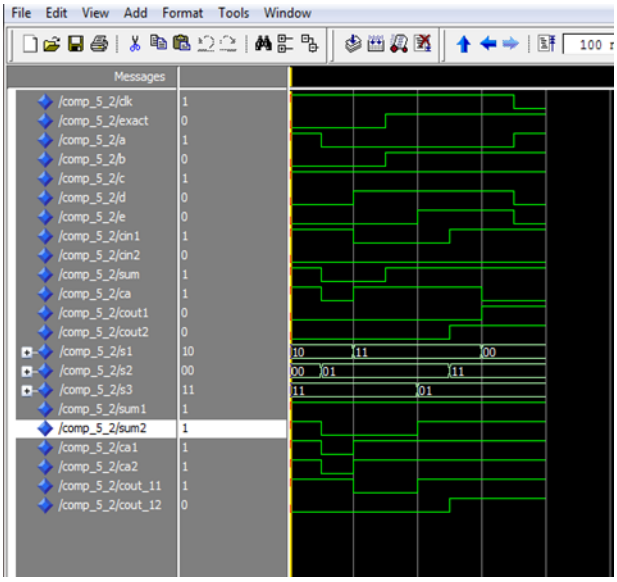


Figure Approximate Multiplier using Dual Quality for 5:2 Compressor

The simulation results are observed for the 8, 16, 32 bits and the comparison table. This16 bit compressor is used in Image processing application. The Power and delay values are calculated in the Tanner EDA tool. The delay and area value generated from Xilinx software for 5:2 compressor. Results of area and power are shown table 4.4 .Finally it is found be efficient in terms of power consumption.

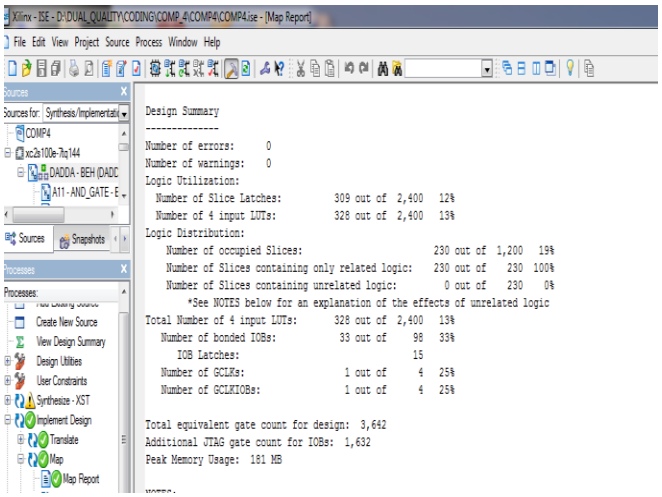
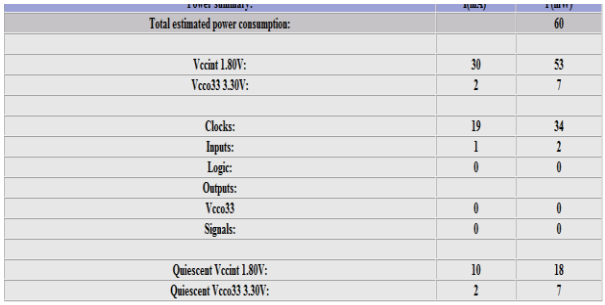


Figure 5:2 Compressor of gate count

Type	PowerDelay	
4-2 compressor using multiplier	0.039watts	24.086ns
5-2 compressor using multiplier	0.022watts	23.338ns

Table Power and Delay value



Total estimated power consumption:		60
Vccint 1.80V:	30	53
Vcco33 3.30V:	2	7
Clocks:	19	34
Inputs:	1	2
Logic:	0	0
Outputs:		
Vcco33	0	0
Signals:	0	0
Quiescent Vccint 1.80V:	10	18
Quiescent Vcco33 3.30V:	2	7

Figure 5:2 Compressor of power consumption

Table Regular Dadda Multiplier

Multiplier N by N	Area (μm^2)	Delay (ns)	Power (µw)	Transistor count
8 by 8	8428	3.40	6.32	1536
16 by 16	29169	4.71	33.09	3148
32 by 32	105237	5.92	210.50	7518
64 by 64	397146	7.54	925.92	14125

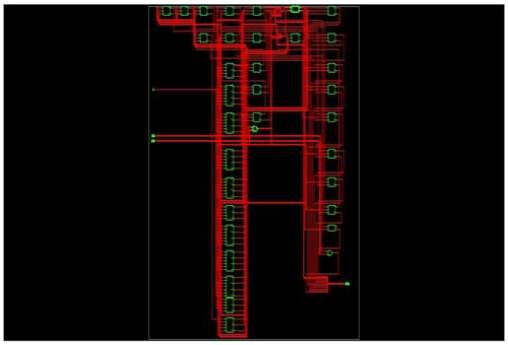


Figure 5:2 compressor using multiplier RTL design

CONCLUSION

Based on all the systems surveyed and their advantages and drawbacks, it presents 5:2 compressor, which had the flexibility of switching between the exact and approximate operating modes. These compressors were employed in the structure of a 8-bit Dadda multiplier to provide a configurable multiplier whose accuracy (as well as its power and speed) could be changed dynamically during the runtime. Future scope for the compressors is to reduce the lower delay and power consumption in the approximate mode compared with those of the recently suggested approximate compressors. When comparing with non-compressor based approximate multipliers; the errors of the proposed multipliers were higher while the design parameters were considerably better. The next could be the multipliers realized based on the suggested compressors compared with the considered approximate multipliers.

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