ISSN:2348-2079

Volume-6 Issue-2

International Journal of Intellectual Advancements and Research in Engineering Computations

A soft switching ZVS sepic inverter topology

B.ShanjeevSurya[1], S.Thirumurugan[2], K.Anbuselvi[3], R.Janani[4], V.Dhinesh[5]
[1234] UG Scholar, [5] Assistant Professor, Department of EEE, Muthayammal Engineering College, Rasipuram, Tamilnadu, India

Abstract— **A novel switching loss reduction technique for three-phase PWM rectifier-inverter topology (Fig. 2) for UPS applications is proposed in this paper. This hybrid topology uses only nine IGBT devices for AC/AC conversion through a quasi d.c. link circuit. this novel switching loss reduction technique will reduce the switching losses and improves the total harmonic distortion of the nine switch inverter. The operating principle of the converter is elaborated and a dedicated advanced space vector modulation scheme is presented. The performance of the proposed converter is verified by simulation on a 5 kVA prototyping UPS system.**

Keywords-**component; - Harmonic distortion, induction motor drives,UPS(uninterrupted power supply) Power conversion efficiency, Pulse width modulation (PWM), space vector, switching loss, voltage source inverter (VSI).**

I.Introduction

Today's power electronics is an enabling technology to overcome the stringent regulation on power utilities. Every year the control techniques have been revised for better control of power converters. Voltage source inverters are popular in range of applications such as motor drives; uninterruptible power supplies (UPS), active rectifiers, and static compensators (STATCOM). Uninterruptible power supply (UPS) is widely used to power equipments in critical applications. Apart from rotary and hybrid UPS that use flywheels to store energy, all static UPS systems which work solely upon electrical energy storage and power electronic converters can be generally classified as three major types: on-line, off-line, and line-interactive [1–3]. An ideal UPS is desired to produce a regulated sinusoidal output voltage for its critical load under any operating conditions, to have seamless transition between normal operation and power failure modes, and to draw sinusoidal input currents from the utility supply with unity power factor. Of all the three types, the online UPS [4-7] characterized by the double-conversion structure provides the best overall performance. Fig. 1a shows the simplified block diagram of an online double-conversion UPS that satisfies the above requirements. It is composed of a PWM rectifier, a PWM inverter, a battery and a static transfer switch. During normal operation, the load is

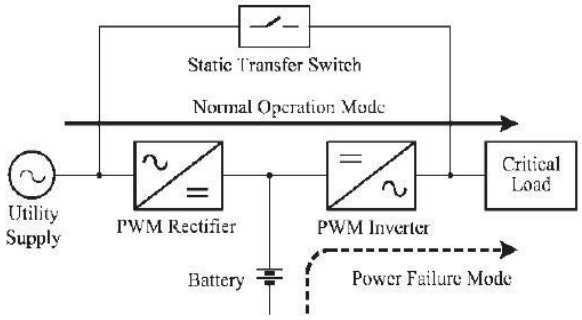


Fig 1. Conventional on- line UPS

powered by the inverter through the rectifier and the utility supply. To maximize the dc bus utilization, the third harmonic added should be one-sixth the amplitude of the fundamental modulating sinusoids (THIPWM6).. The PWM rectifier normally operates with a unity power factor and low line current distortion, while the inverter delivers a highquality regulated supply to its critical load. Since the load is always supplied by the inverter, no mode transition time is required. However, although the online type UPS possesses all the above mentioned benefits, it is also the most expensive solution of all because its configuration requires two power conversion stages, which increases the manufacturing cost and power losses. Line-interactive UPS [8-11] and off-line UPS [12-13] provide cheaper and more efficient solutions, but can only offer inferior performance in terms of power conditioning and mode transitions. Recent researches can be found aimi ng at improving performance as well as reducing the cost of UPS systems. In order to meet power grid requirements on the line side, better harmonic profile and power factor control capability has been one of the main focuses [14-15]. It should be mentioned that even multilevel converters have been proposed for use in UPS to improve the input/output waveform quality [16]. On the other hand, a number of designs have been proposed to reduce the cost of UPS systems, such as a single-converter UPS with filtering capabilities [17], a line-interactive UPS that can act as a voltage stabilizer [18], and a three-phase series-parallel topology with reduced part count [19].

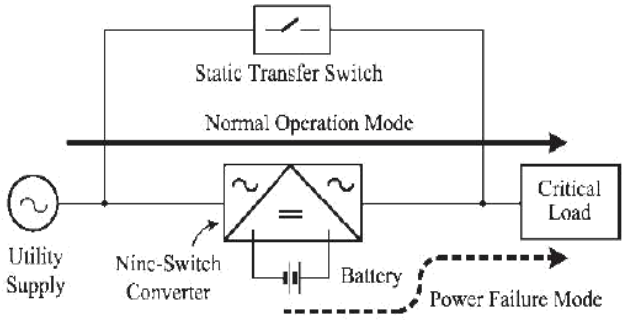


Fig 2. Proposed on line ups

But these systems either cannot adjust the line current, input power factor, and load voltage simultaneously or involve complex structure and control. This paper proposes a novel nine-switch converter topology for online UPS applications. As shown in Fig. 1b, the proposed UPS system has a simple and balanced structure which contains only one power conversion stage. Under normal operation, the power is delivered to the critical load partially through ac/ac direct conversion and partially through the dc circuit. When the utility power fails, the battery in the dc circuit delivers power to the load. Compared with the PWM back-to-back converter that employs 12 active switches, the proposed converter only uses nine switches, leading to the reduction of manufacturing cost as well as device power losses. In addition, the proposed UPS system features regu- lated sinusoidal inputs and outputs, unity input power factor, and seamless transition between the normal operation and power failure

II. SWITCHING SEQUENCES AND ITS CONSTRAINTS

The voltage vectors, produced by a three-phase inverter, divide the space vector plane into six sectors as shown in Fig. As the sectors are symmetric, the discussion here is limited to sector I alone. In the space vector approach to PWM, an average vector equal to the sample of the reference vector is generated in every subcycle or sampling period T_S. Given a commanded vector of magnitude V_{REF} and angle in sector I as shown in Fig. 1, the volt-second balance is maintained by applying the active state *1*, the active state *2* and the two zero states together for durations T_1, T_2 and T_Z, respectively, as given in (1).

$$T2 = \overline{V}ref \sin(\alpha) * Ts/\sin(60^0)$$

$$Tz = T1\text{-}T2\text{-}Ts \qquad \text{- } (1)$$

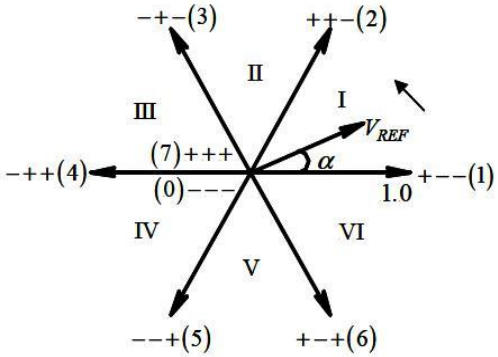


Fig .3 Voltage vectors of a VSI. Magnitudes of the vectors are normalized with respect to dc bus voltage V_{dc} . I–VI are sectors.

With space-vector-based PWM, for any given $\boldsymbol{V}_{\mathbf{REF}}$ insector I, the conventional switching sequence starts with one zero state and ends with the other, i.e., 0127 (or 7210), as indicated in Fig. 4(a). The clamping sequences 012 (or 210) and 721 (or 127) use only one zero state, as shown in Fig. 4(b) and (c), respectively. Special sequences, illustrated in Fig. 4(d)–(g), also employ only one zero state (say 0), but apply its neighboring active state (say 1) twice in the given subcycle for a total duration specified by (1). Sequences 0121 (or 1210) and 7212 (or 2127), shown in Fig. 4(d) and (e), respectively, have been introduced in the context of low switching frequency PWM techniques for high-power induction motor drives in [9]. Subsequently, these have been studied for applications where the inverter switching frequency is much higher than the fundamental modulating frequency in [11] and [16]. Sequences 1012 (or 2101) and 2721 (or 1272), illustrated in Fig. 4(f) and (g), respectively, have been reported more recently in [14] and [17]. While a phase cannot switch more than once in a half-carrier cycle with triangle-comparison-based PWM, a phase switches twice in a subcycle when special sequences are employed in space-vector-based PWM generation [14], [17]. The Y-phase switches twice when sequences 0121 and 7212 are employed. With sequences 1012 and 2721, respectively, R-phase and B-phase switch twice. Also, one of the phases is clamped with any special sequence. Hence, these sequences are also known as *double-switching clamping sequences* [14], [16]. When clamping sequences and/or special sequences are employed, the switching frequency of a phase varies over a line cycle. The switching frequency, averaged over a line cycle, is termed *average switching frequency* f_{SW} [14], [16]. The criterion of "equal average switching frequency" is used for comparison of various PWM techniques in this paper.

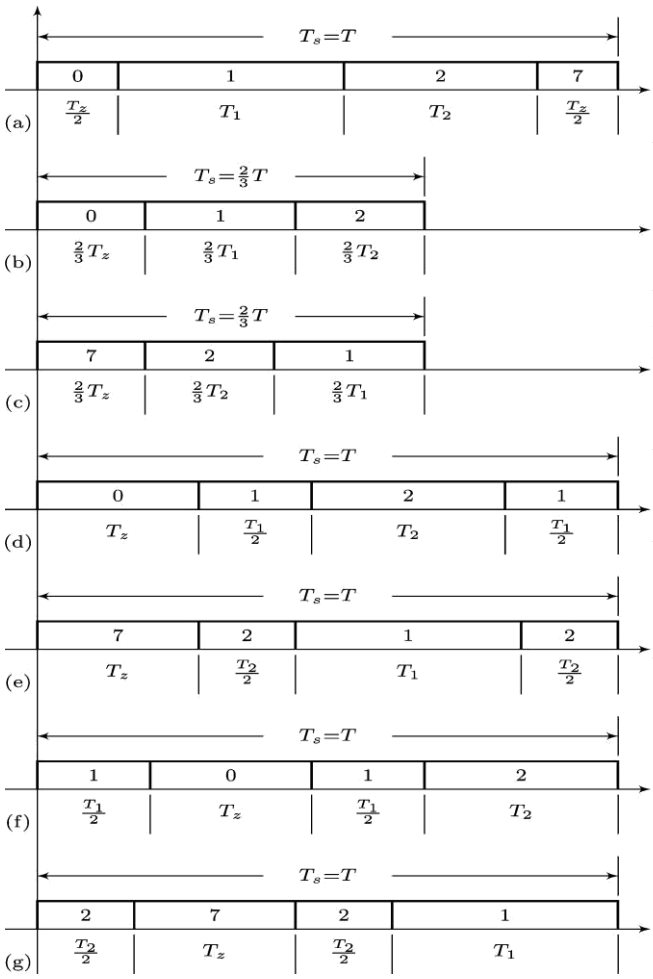


Fig. 4 Seven possible switching sequences in sector I: (a) 0127, (b) 012, (c) 721, (d) 0121, (e) 7212, (f) 1012, and (g) 2721.

Switching constraints and SVM scheme

In the nine-switch topology, the input and output voltages of the converter are independently controlled through the three switches per leg. The proposed converter has only three valid switching states per phase as illustrated in Table I, where v_{AN} and v_{XN} are the voltages at nodes *A* and *X* with respect to the negative dc bus *N*. When switches S_1 and S_2 in the left leg of the converter are turned on and switch S_3 is turned off, $v_{AN} = v_{XN} = V_d$.With S_1 turned off, and S_2 and S_3 turned on, $v_{AN} = v_{XN} = 0$. If the middle switch S_2 is be higher than v_{AN} at any time, i.e. v_{XN} v_{AN}.

Switching State	S_1	S_2	S_3	v_{AN}	v_{XN}
1	On	On	Off	v_d	v_d
2	Off	On	On	0	0
3	On	Off	On	v_d	0

Table 1. Switching states and converter leg voltages

off and the other two switches are on, $v_{AN} = V_d$ and v_{XN} = 0. It can be concluded that the main constraint for switching scheme design is that the converter leg voltage v_{XN}, cannot To satisfy this constraint, a special space vector modulation (SVM) scheme is developed to operate the converter. As illustrated in Fig. 3a, the space vector diagram for the nine-switch converter is no different from that of the conventional PWM back-to-back converter. For the space vectors, a 'P' indicates that the corresponding phase leg output is connected to the positive dc bus and outputs V_d whereas an 'O' denotes that it's been switched to the negative dc bus and the output is zero. Under CF mode operation, the voltage reference vectors for the rectifier and inverter $V_{R,ref}$ and $V_{I,ref}$ are both rotating in the space with the same angular velocity of . In order to guarantee that v_{XN} will not be higher than v_{AN} during a sampling period T_s, common-mode offsets should be added to push t e rectifier modulating waves to the top of the dc plane and to shift the inverter modulating waves to the bottom. This arrangement is shown in Fig. 3b where synthesized modulating waves for both converters with different modulation indices are plotted. In the figure, m_r and m_i are the rectifier and inverter modulation indices for dc voltage and inverter output voltage adjustment, respectively. Taking Sector I as an example, the switching patterns for the rectifier and inverter in a whole sampling period are presented in Fig. 3c and 3d. The popular seven-segment SVM switching sequence with centered pulse placement is adopted. The dwell times for the stationary vectors are calculated y

$$\begin{cases} T_a = T_s m_a \sin\left(\dfrac{\pi}{3} - \theta\right) \\ T_b = T_s m_a \sin\theta \\ T_0 = T_s - T_a - T_b \end{cases}$$

where ma represents the modulation index for either rectifier or inverter. On the rectifier side, dc offset is added by using as muchas possible the PPP zero vector over the *OOO*. Compared with the conventional seven-segment SVM which evenly distributes the zero vectors, here a maximum possible percentage is converted from *OOO* to *PPP*, as illustrated by the shadowed portion *T* in Fig. 3c. Since the added offset must be constant over the entire fundamental cycle and because the exact amount of *T* can befound

$$T_0 = T_s\left[1 - m_a \sin\left(\frac{\pi}{3} - \theta\right) - m_a \sin\theta\right] \geq (1 - m_a)T_s$$

as

$$\Delta T = \frac{1}{4}(1 - m_a)T_s$$

Similarly, for the inverter, *OOO* is used as much as possible for the zero vectors (Fig. 3d). This is done by converting the same amount of *T* as given in Eq.(3) from PPP to *OOO*, ensuring that the inverter's modulating waves are shifted to the bottom of the dc plane. It should be pointed out that although the instant value of v_{AN} is always higher than v_{XN} during any sampling period, this does not necessarily mean that the fundamental comp nent of the inverter output voltage v_{XY} should be lower than that of the rectifier inputvoltage V_{ab} . Because the rectifier's phase voltages are never lower than the inverter's, the theoretical instantaneous magnitude of the CMV is 0, – $V_d/3$, – $2V_d/3$ or – V_d. However, since a – V_d CMV only occurs when rectifier is switched to PPP while inverter is at *OOO*, it will not appear in normal operating conditions due to the synchronous rotation of the rectifier and inverter reference vectors, unless the inverter modulation index is too low such that the longest pulse on v_{XN}, v_{YN} and v_{ZN} is narrower than the shortest pulse on v_{AN}, v_{BN} and v_{CN} during a single sampling period.. It is evident that the modulation scheme satisfies the special switching constraint for the nine-switch converter topology while the two modulation indices for the rectifier and inverter can be adjusted from zero to unity fully independently.

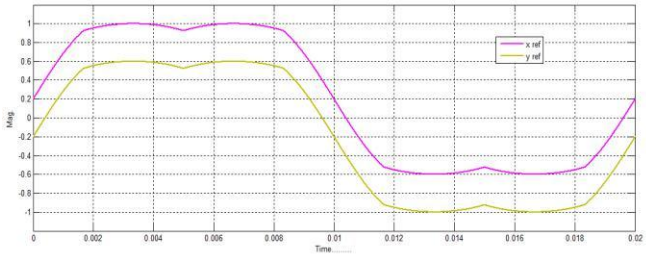


Fig 5.SVM modulation waveform

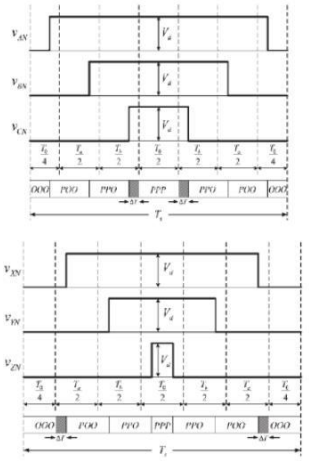


Fig 6.Switching pattern for rectifier and Switching pattern for inverter

Fig. 4 shows the simulated waveform of the rectifier PWM voltage v_{AB} and its harmonic spectrum when the converter operates with a supply voltage of 208 V (line-to-line, 60 Hz) and dc voltage of 320 V. The switching frequency of the converter is 3240 Hz, and the rectifier modulation index mr is 0.9. The harmonic spectrum in Fig. 4b shows that the rectifier PWM waveform does not contain any low order harmonics, and the dominant harmonics are centered around converter switching frequency of 3240 Hz, the same attributes as the conventional sinusoidal modulation.

Fig. 5 shows the simulated waveform and spectrum of the inverter output voltage v_{XY} with a fundamental frequency of 60 Hz. It is interesting to note that the inverter output voltage waveform, its fundamental component, and THD are very close to those of the rectifier given in Fig. 4. Fig. 5c illustrates the THD curve of the inverter output voltage v_{XY} versus the inverter modulation index mi of the nine-switch converter. The THD curve of the output voltage of the PWM back-to-back converter operating at the same switching frequency is also plotted. It can be noted that the voltage harmonic performance of the nine-switch converter is similar to that of its counterpart The system has a power rating SR of 5 kVA and the inverter's modulation index is 0.9, the converter is working in CF mode with other system parameters being the same as those used in the previous section. A PWM back-to-back converter is simulated with identical parameters to provide a comparison. In the figure, Ptop, Pmid and Pbot designate respectively the power losses on the top, middle and bottom three switches in the nine-switch converter; whereas $P_{rec\text{-}u}$, $P_{rec\text{-}l}$, $P_{inv\text{-}u}$ and $P_{inv\text{-}l}$ denote the losses in the PWM back-to-back converter, representing those from the upper and lower switches in the rectifier, upper and lower switches in the inverter, respectively. It can be seen from Fig. 6 that, unlike the back-to-back converter

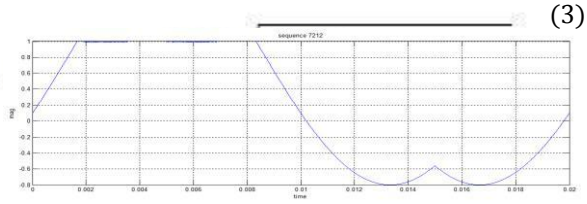
which features a balanced loss distribution on the upper and lower switches, the loss distribution in the nine-switch converter is not even. In the nine-switch converter, due to the fact that power is partially transferred directly through the switches, the middle . three devices are subject to higher current stress and produce more power losses than the top and bottom three devices. However, the nine-switch converter still possesses an advantage over the backto- back converter in terms of the total semiconductor loss, which is 1.62 % of the system's rated power, comparing to its counterpart's 2.43 %

III.INFLUENCE OF SEQUENCES ON INVERTER SWITCHING LOSS

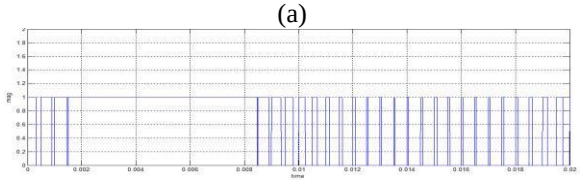
Considering R-phase, the switching energy loss per subcycle in the R-phase leg is proportional to dc bus voltage, device switching times, and the R-phase current. Only the fundamental component of R-phase current $i_{R,1}$ need be considered since the contribution of ripple current to this energy loss is insignificant [6]. The switching energy loss is also proportional to the number of switching's of R-phase in the given subcycle n_R, which depends on the switching sequence used [17]. For comparative evaluation of sequences, one could simply consider the product of $i_{R,1}$ and n_R to be a measure of the energy lost due to switching in this phase.

$$P_{SW} = \frac{1}{2}\int_{\phi}^{\pi+\phi} P_{SUB,PH}\, d\omega t. \quad (2)$$

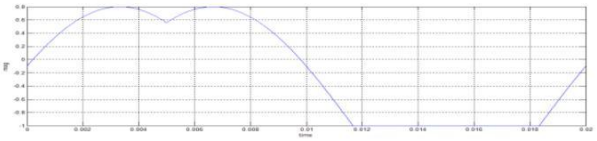
(3)



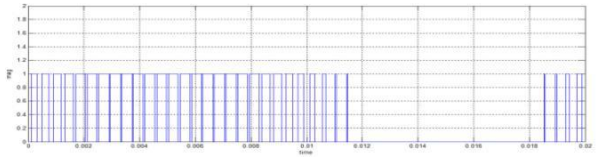
(a)



(b)



(c)



(c)

Fig 8 Modulating waves for 7212 and 0121 (a) and (c) respectively; its corresponding pulse (b) and (d)

The switching energy loss is also proportional to the number of switching of R-phase in the given subcycle nR, which depend on the switching sequence used. For comparative evaluation of sequences, one could simply consider the product of |iR,1 | and nR to be a measure of the energy lost due to switching in this phase. Energy lost due to switching in R phase = iR,1* nR Where, iR,1=fundamental component of R phase current(A) nR=number times switching in R phase

The condition based novel switching sequences are detailed in this chapter .The application of the novel sequence (0121 and 7212) in SVM based inverter, the switching losses gets reduced for about 22 to 24%

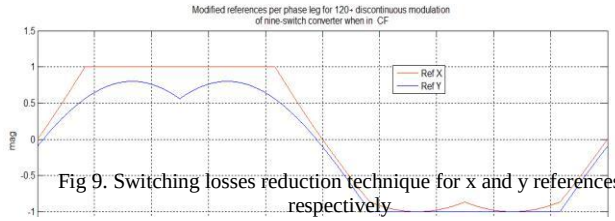


Fig 9. Switching losses reduction technique for x and y references respectively

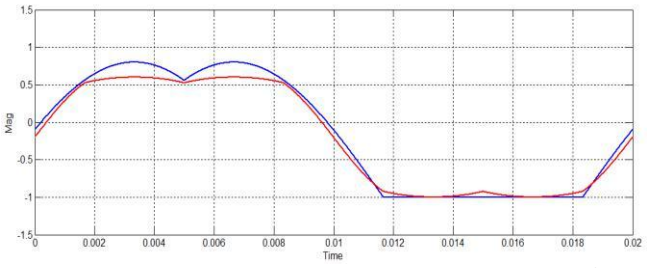


Fig 10. Hybrid Switching loss and THD reduction technique for x and y
referemce respectively

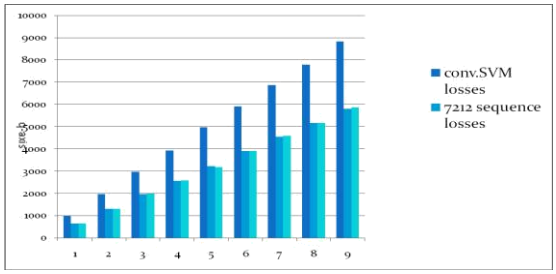


Fig. 10 Comparison of switching losses with conv.SVM ,0121 and 7212

IV.Nine-switch converter topology and modulation

Fig. 2 shows the proposed three-phase nine-switch converter topology. This converter has three legs with three switches per leg. The novelty of this converter is that the middle switch in each of the three converter legs is shared by the rectifier and inverter, thereby reducing the switch count by 33 % in comparison to the PWM back-to-back converter. The utility power is delivered to the load partially through the middle three switches (direct ac/ac conversion)
and partially through a quasi dc link circuit.

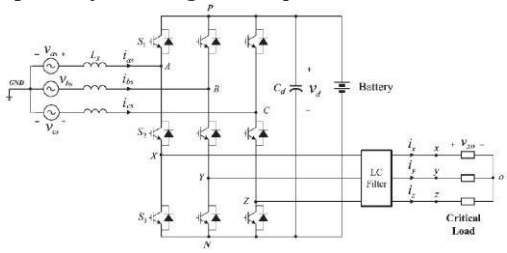


Fig 11. Hybrid topology for nine switch rectifier-inverter topology

For the convenience of discussion, we may consider that the rectifier of the nine-switch converter is composed of top three and middle three switches whereas the inverter consists of middle three and bottom three switches.
The converter has two modes of operation: 1) constant frequency (CF) mode, where the output frequency of the inverter is constant and also the same as that of the utility supply while the magnitude of the inverter output voltage is adjustable, and 2) variable frequency (VF) mode, where both magnitude and frequency of the inverter output voltage are adjustable [20]. The CF mode of operation is particularly suitable for applications such as UPS systems whereas the VF mode can be applied to variable-speed drives. In this paper, only the CF mode is presented for UPS applications.

Table II: System parameters and testing conditions

Supply Voltage	Line Inductance	DC Voltage	DC Capacitance	Output LC Filter		Load Resistance
				Capacitance	Inductance	
208 V(Line to Line, 60Hz)	2.5 mH	320 V	9400 μF	31 μF	2.5mH	8.2

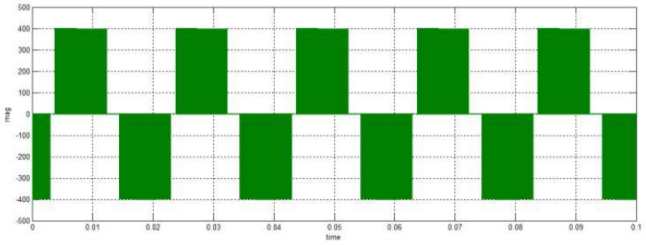


Fig 12.Upper line to line output voltage with the upper Modulation index ma=0.9 and measured voltage is V upper(rms) =370 volts

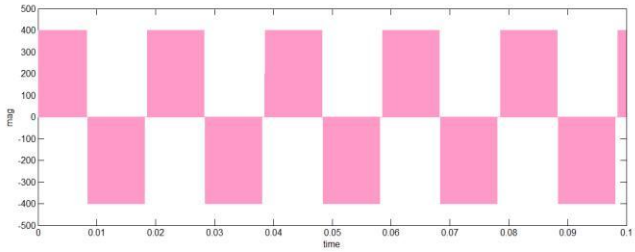


Fig 13. Lower line to line output voltage with the lower Modulation index ma=0.82 and measured voltage is V lowerr(rms) =310 volts

V.Conclusion

The novel switching losses reduction technique base nine-switch PWM rectifier-inverter topology is proposed in this paper for three-phase online uninterruptible power supplies. This hybrid topology uses only nine IGBT devices for AC to AC voltage conversion through a quasi dc link circuit .The hybrid switching loss reduction technique employs different switching sequence or the discontinuous and continuous modulation scheme. This technique reduces the switching losses about 22 to24 % . The proposed topology has a feature of reduction in switch count ,reduced switching loss and lower THD than SVM from fig 10.. It is particularly suitable for online UPS applications, due the reduced switching losses it leads to design of compactness in power converter due to the reduced size of heat sinks The performance of the converter topology is verified through simulation and experiments on 5 kVA prototyping UPS system.

VI. References

[1] S. Karve: Three of a kind - UPS topologies and IEC standard, IEE Review, Volume 46, Issue 2, pp 27-31, March 2000.

[2] S. B. Bekiarov and A. Emadi: Uninterruptible power supplies: classification, operation, dynamics, and control, in IEEE Applied Power Electronics Conference and Exposition, 2002.

[3] J. M. Guerrero, L. Garcia de Vicuna, and J. Uceda, "Uninterruptible power supply systems provide protection," IEEE Industrial Electronics Magazine, vol. 1, no. 1, pp. 28-38, 2007.

[4] V. M. Pacheco, L. C. de Freitas, J. B. Vieira, Jr., A. A. Pereira, E. A. A. Coelho, and V. J. Farias: An online no-break with power factor correction and output voltage stabilization, IEEE Trans. Power Electron., vol. 20, no. 5, pp. 1109-1117, 2005.

[5] T. H. Abdelhamid, M. K. Darwish, P. Mehta, A. L. Mohamadien, and M. S. Abo-Elela: A new flexible and compact high-frequency link on-line UPS system, EPE Journal, vol. 5, no. 2, 1995.

[6] M. A. De Rooij, J. A. Ferreira, and D. Van Wyk: A novel unity power factor low-EMI uninterruptible power supply, IEEE Trans. Ind. Appl., vol. 34, no. 4, pp. 870-877, 1998.

[7] A. Nasiri, N. Zhong, S. B. Bekiarov, and A. Emadi: An On-Line UPS System With Power Factor Correction and Electric Isolation Using BIFRED Converter, IEEE Trans. Ind. Electron., vol. 55, no. 2, pp. 722-730, 2008.

[8] F. Kamran and T. G. Habetler: A novel on-line UPS with universal filtering capabilities, IEEE Trans. Power Electron., vol. 13, no. 3, pp. 410-418, 1998.

[9] B. H. Kwon, J. H. Choi, and T. W. Kim, "Improved single-phase line-interactive UPS," IEEE Trans. Ind. Electron., vol. 48, no. 4, pp. 804-811, 2001.

[10] P. Fu-Sheng and H. Shyh-Jier: A novel design of line-interactive uninterruptible power supplies without load current sensors, IEEE Trans. Power Electron., vol. 21, no. 1, pp. 202-210, 2006.

[11] H. L. Jou, J. C. Wu, C. Tsai, K. D. Wu, and M. S. Huang: Novel line-interactive uninterruptible power supply, Electric Power Applications, IEE Proceedings-, vol. 151, no. 3, pp. 359-364, 2004.