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Design of area efficient fault tolerant parallel FFTS using partial summation and parallel correction

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Abstract:

In signal processing and communication systems, digital filters are widely used. It is common to find several filters or FFTs operating in parallel. In some cases, soft errors pose a reliability threat to modern electronic circuits. Fault tolerant filter implementation needed. Several protection schemes have been proposed to detect and correct errors in FFTs. for some applicationABFT techniques used. The error it can be detected and corrected by using algorithmic properties, signal processing and communication applications are well suited for ABFT.In this brief, initially this technique is first applied to protect FFTs then the improved protection schemes that combine the use of ECC and Parseval checks are proposed and evaluated for the multiple error corrections. The result shows that the new schemes can further reduce the implementation cost and provide low complexity.

Keywords: Algorithmic-Based Fault Tolerance (ABFT), Error Correction Codes (ECC), Fast Fourier Transforms (FFTs), Parseval theorem, Soft errors.

I.INTRODUCTION

Digital filters are widely used in signal processing and communication system. In some cases, the reliability of those systems are critical and fault tolerant filter implementations are needed. Fault tolerance is the realization that always have faults (or the potential for faults) in our system. Need to design a system in such a way that it will be tolerant of those faults. That is, the system should compensate the faults and continue to function. This can be achieving by redundancy. This need is further increased by the intrinsic reliability challenges of advanced CMOS technologies. Soft errors it can change the logical value of a circuit node creating a temporary error that can affect the system operation. While using filters in parallel soft errors are vulnerable to the circuits. FFT, it plays an important role in digital signal processing. Aninteresting option is to use algorithmic based fault tolerance (ABFT) technique [3] that try to exploit the algorithmicproperties to detect and correct errors. When the circuit to be protected has algorithmic orstructural properties a better option can be to exploit those properties to implement fault tolerance.

II.EXISTING TECHNIQUES USED

In the protection of parallel FFTs, it is assumed that there can only be a single error on the system at any given point

in time. This is acommon assumption when considering the protection against radiation-induced soft errors [4].

1. Protection using ECCs

A General scheme based on the use of error correction codes (ECCs) has been used. This technique can be used for operations, in which the output of the sum of several inputs is the sum of the individual outputs [1].

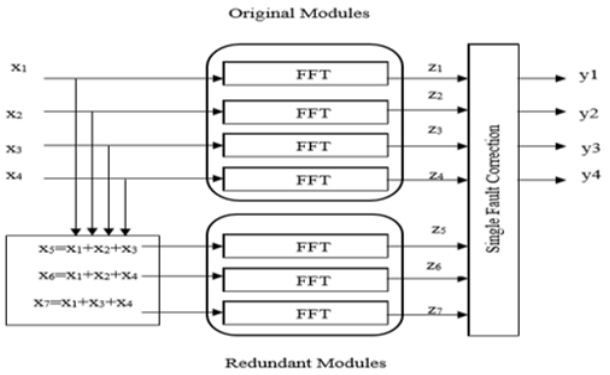


Fig 1: Parallel FFT protection using ECCs.

In a parallel FFT protection using ECCs it has two types of Modules namely original modules and redundant modules. Redundant modules used for detect and correct the errors. This scheme isshown inFig.1.In this example simple single errorcorrectionHamming code [2] isused. The error it can determined by using observed differences on each of the check theinput. For the first redundant module is and the DFT is a linear operation

$x5 = x1 + x2 + x3_{(1)}$

Its output z5 can be usedto check that,

$z5 = z1 + z2 + z3$ (2)

This will be denoted as c_1 check. Compare to the TMR based technique the overhead of the technique is lower [1].

2. Protection using parity-SOS

Many techniques have been proposed to protect the FFT,One of them is the Sum of Squares (SOSs) check [3] that can

be used to detect errors. The SOS check is based on the Parseval theorem that states that the SOSs of the inputs to the FFT are equal to the SOSs of the outputs of the FFT except for a scaling factor. For parallel FFTs, the SOS check can be combined with the ECC approach to reduce the protectionoverhead. The SOS check can only detect errors,

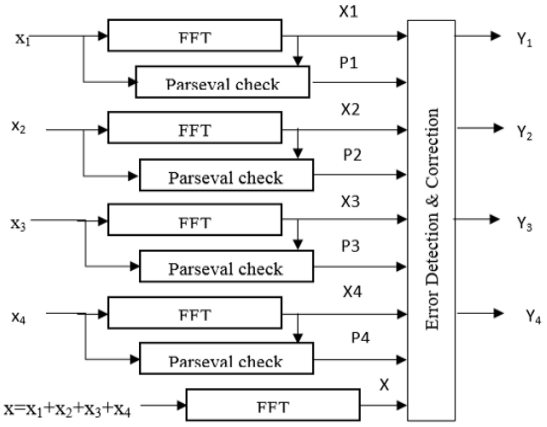


Fig 2: Parallel FFT protection using parity-SOS.

The ECC part implement the correction. A redundant (the parity) FFT is added that has the sum of the inputs to the original FFTs as input. An SOS check is also added to each original FFT. In case an error is detected (using P1, P2, P3, P4), the correction can be done by recomputing the FFT in error using the output of the parity FFT (X) and the rest of the FFT outputs.

$$X1c = X - X2 - X3 - X4 \quad (3)$$

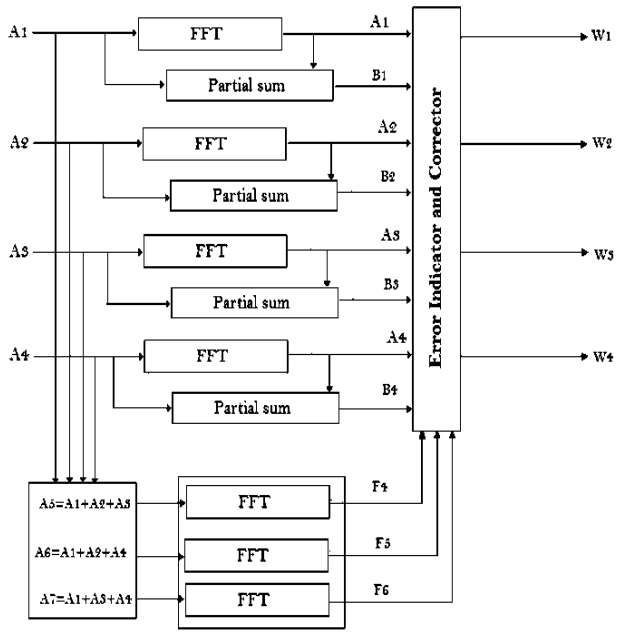
3. Parity-SOS-ECC Method

The Parity-SOS-ECC based fault tolerant technique is the Combination of the previous two techniques. Combine the SOS check and the ECC approach is instead of using anSOS checkper FFT, use anECC forthe SOSchecks. In this method, Parseval check is used to detect and correct theerrors. The main advantage of this method is number of Parseval check is less compared with previous.

III.PROPOSED METHOD

1. Partial Summation

In this proposed method partial summation technique were useful for the multiple error detection and correction. In this previous existing methods it can able to correct single FFT at the time. For example if error occurs in A1it will able to correct the error. If error occurs in A1and A2 we can't able to correct the errors by the existing technique. The proposed work focuses on new technique for reducing the hardware overhead and increasing the error correction capability.The new technique which focuses on the existing systems limitations. The technique analyzed in the previous work has certain limitation due to the complexity of handling larger number of FFTs and Sum of Squares block. Instead of using Sum of Squares, Partial summation is used for calculatingits parity at the input and the output side of the FFT.It sums all possible node values of 4-point FFT



along with the twiddle factors.

Fig 3.Parallel FFT protection using partial summation

Multiplication operation which leads to the complexity in Sum of Squares is thus eliminated using only the adder blocks. Technique 1 also uses 3 parallel redundant FFT in thecase of 4-parallel FFT design for correcting multiple errors in fault tolerant for soft error. Partial Summation block for less error prone applications. For example when the error occurs in A1 and A2 then it can be detected by the partial summation used individually for FFT blocks. The first check equation is selected in such a way that the both error block signals are not present.

$$A5=A1+A2+A3 \quad (4)$$

$$A6=A1+A2+A4 \quad (5)$$

$$A7=A1+A3+A4 \quad (6)$$

The error in first FFT is corrected by using equation (6) as

$$B1=B7-B3-B4 \quad (7)$$

Once the error is detected using in the first FFT is corrected then equation (4) can be used for correcting error in the second onewhich is given as,

$$B2=B5-B1-B3 \quad (8)$$

The Partial Summationreduces the number of additional squaring blocks and also reduces the shelter overhead. In our implementation those blocks are protected with adders used to compute the inputs and the outputs to the redundant FFTs in the existingtechnique with a small impact on circuit complexity as they are much simpler than the FFT computation.

2. Parallel Correction

In this method, we are using Parseval check method to detect the errors in the original module. By using this method we can able to detect more than one error in the original module. After that errors in the original modules are corrected by using ECC.In Fig4 partial summation block will replaced by Parseval check for performing parallel correction method.

IV.RESULTS

The existing techniques and proposed method results obtained by using tools like ModelSim and Xilinx. In the proposed method the errors present in the original module FFTs it can be detected by using parallel correction.The detected error in can be corrected by using ECC approach as a redundant module. In Fig 4 it shows the error part, Fig 5 it shows the corrupted part detection after that final corrected output shown in Fig 6.

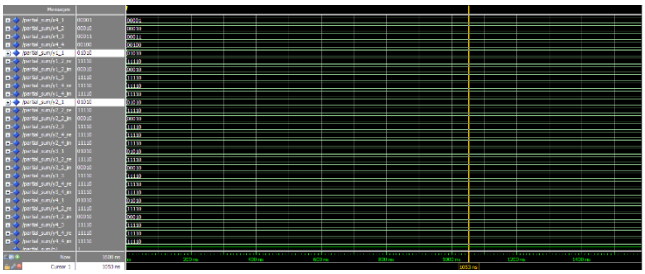


Fig 4-Error Part

Fig 5-Corrupted Part.

Fig 6-Final output.

Fig 7-OFDM Application output using parallel correction

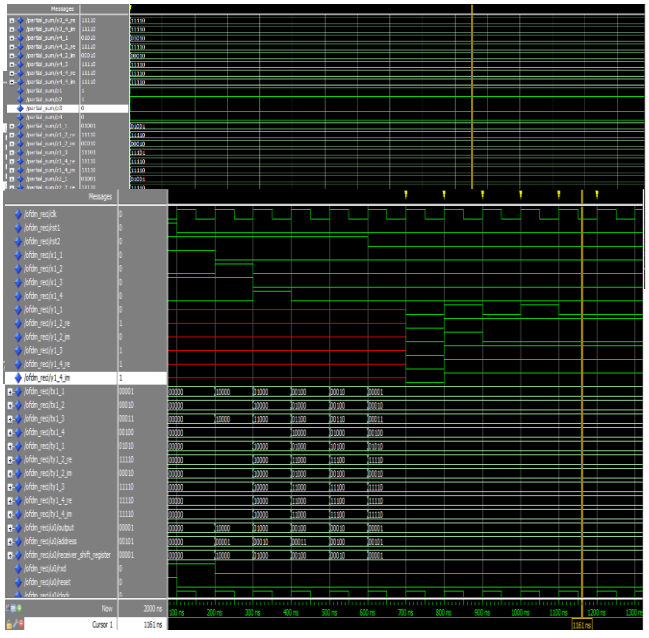


Table 1: Comparison Table -Existing and Proposed method

V.CONCLUSION

Final observation from existing techniques that the ECC scheme can detect all errors on the other hand the SOS check detects most errors but does not guarantee the correction of all errors. The combination of ECC and Parseval check technique it can able to achieve the lowest overhead among those three existing techniques. Additionally it has advantage of the combination of (ECC & Parseval check) this method efficient area usage. Those three existing techniques it's useful for single FFTerror correction only. For handling multiple FFTs at the time partial summation method and parallel correction methods were useful. It also achieves the efficient area usage. That parallel correction structure it applied in the OFDM applications in the transmitter side.

Advantages:

- Low implementation complexity.
- Multiple error protection.

Applications:

- MIMO-OFDM systems.
- Filter banks.

TECHNIQUES	AREA (Gates used)	Delay (ns)	Power (mW)
ECC	16735	3.346	263
Parity-SOS	10561	3.969	253
Parity-SOS-ECC	9584	3.249	252
Partial Summation	6948	5.051	246
Parallel Correction(OFDM)	3101	2.205	243

- Wireless Applications.

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