



A survey on real time electrical capacitance tomography using VLSI architecture

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Abstract- This paper presents a fixed-point reconfigurable parallel VLSI hardware architecture for realtime Electrical Capacitance Tomography (ECT). It is modular and consists of a front-end module which performs precise capacitance measurements in a time multiplexed manner using Capacitance to Digital Converter (CDC) technique. Another FPGA module performs the inverse steps of the tomography algorithm. A dual port built-in memory banks store the sensitivity matrix, the actual value of the capacitances, and the actual image. A two dimensional (2D) core multiprocessing elements (PE) engine intercommunicates with these memory banks via parallel buses. A Hardware-software codesign methodology was conducted using commercially available tools in order to concurrently tune the algorithms and hardware parameters. Hence, the hardware was designed down to the bit-level in order to reduce both the hardware cost and power consumption, while satisfying real-time constraint. Quantization errors were assessed against the image quality and bit-level simulations demonstrate the correctness of the design. Further simulations indicate that the proposed architecture achieves a speed-up of up to three orders of magnitude over the software version when the reconstruction algorithm runs on 2.53 GHZ based Pentium processor or DSP Ti's Delphino TMS320F32837 processor. More specifically, a throughput of 17.241 Kframes/sec for both the Linear-Back Projection (LBP) and modified Landweber algorithms and 8.475 Kframes/sec for the Landweber algorithm with 200 iterations could be achieved. This performance was achieved using an array of $[2 \times 2] \times [2 \times 2]$ processing units. This satisfies the real-time constraint of many industrial applications.

Index Terms—ECT, FPGA, matrix multiplication decomposition.

I.INTRODUCTION

Electrical Capacitance Tomography (ECT) is an effective technique to measure a process non-intrusively by reconstructing the 2D or 3D dielectric distribution of its different constituencies [1][2][3]. This makes ECT a good candidate for several industrial applications such as two-phase flow monitoring, quality control in manufacturing industry, and corrosion detection [4]. In the last few years, several ECT systems have already been

suggested [1]. Most of them used a desktop computer as a main processing unit and focused their research mainly on improving the accuracy and execution time of the algorithms on general purpose computers. Nevertheless, the tremendous computation complexity of the tomography algorithms let them to be executed still relatively slowly (in few seconds order), preventing them to sustain real-time applications. Hence, only few research works have been done on designing dedicated hardware architectures for ECT tomography using either DSP

processor or FPGA technology. In [5], a dedicated architecture based on the DSP processor, TMS320C6701, operating at 133 MHz was suggested for the image reconstruction algorithm. The system consists of 12 electrodes and claimed to be able to achieve the image reconstruction of images of 480 pixels within a throughput of 135 frames/s, when using the Linear Back Project (LBP) algorithm. Similarly, in [6] a TMS3206416 processor was used in LBP-based ECT system with 16 electrodes to achieve a throughput of 200 frames/s.

The usage of FPGA instead of DSP processors by other researchers was motivated by the fact that FPGA can host a good portion of the control/data flow of the reconstruction algorithm, without the need of series of sequential memory accesses. Hence, recently, an FPGA-based Electrical Impedance Tomography (EIT) system was disclosed in [7]. The system comprises several FPGA-based Impedance Measurement Modules (IMM) comprising independent current sources and voltmeters intercommunicating through a reconfigurable FPGA-based Intra-network controller. Hence, the system could achieve a throughput of around 100 frames/second. The relatively low performance of the system can be justified by the fact that the IMMs modules are mainly involved in data acquisition and electric current generation for the electrodes, rather than in the image reconstruction task itself. Another similar FPGA-based ECT device was disclosed to digitally modulate (i.e. amplitude and phase modulations) the ac signal with various carrier frequencies and let the receivers to band-pass filter the transmitted signal to their allocated carrier frequency [8]. This allows simultaneous data acquisition as well as avoiding the usage of CMOS analog switches.

Other works were also suggested for FPGA-based image reconstruction targeting other tomography modalities such as computed tomography (CT) [9] and Single-Photon Emission Computed Tomography (SPECT) [10]. In [10], a dedicated architecture for SPECT imaging using a scalable multicore onChip Architecture for on-chip communication was proposed. The hardware which consists of 128 processing elements mapped onto an FPGA module could achieve a speed-up by a two orders of

magnitude over 2 GHz Intel core 2 Duo Processor by exploring the intrinsic fine parallelism exhibited by the corresponding algorithm. A reconfigurable and modular interconnection switching network was used to dynamically and arbitrarily interconnect the processors array by eliminating data starvation. Other architectures using Graphics Processing Unit (GPU) for SPECT Tomography were also suggested by exploring their significant performance for arithmetically intensive algorithms that have structured data accesses and limited branching, which is the case of SPECT tomography algorithms [11]. However, compared to FPGA, their performance was lower because of the frequency and randomness of memory access which was off-chip. In [12], a Spartan 6 FPGA-based system for Dual Head Positron Emission Tomography (PET) was used to fully implement the constant fraction discriminator (CFD) algorithm to achieve time-resolution higher than the sampling period. The system consists of a 32-bit DSP RISC processor, running at 66.67 MHz, interfaced with a custom core to perform event timing, energy determination-discrimination, position determination, and coincidence processing in real-time.

In this paper, we present a new architecture of ECT tomography algorithm using FPGA technology. The architecture is flexible enough to host three computationally intensive reconstruction algorithms, namely the LBP, Landweber, and modified-Landweber algorithms. It explores some of the new features of recent FPGA devices such as the DSP blocks and the Block RAM (BRAM). A simultaneous matrix-level and bit level designs was conducted to finely reduce the hardware cost and power consumption, while keeping the overall execution of the algorithms low.

To the best of the authors' knowledge, this is the first embedded system which explores the intrinsic parallelism which is available in modern FPGA for ECT tomography. Extensive simulations indicate that the proposed architecture achieves a speed-up of up to three orders of magnitude over the software version when the reconstruction algorithm runs on 2.53 GHz-based Pentium processor. More specifically, a throughput of 17.241 Kframes/sec for both the Linear-Back Projection (LBP) and modified

Landweber algorithms and 8.475 Kframes/sec for the Landweber algorithm with 200 iterations could be achieved. This performance was achieved using an array of $[2 \times 2] \times [2 \times 2]$ processing units. This satisfies the real-time constraint of many industrial applications.

II RELATED WORKS

2.1 “Image reconstruction algorithms for electrical capacitance tomography”,[1]

Electrical capacitance tomography (ECT) is used to image cross-sections of industrial processes containing dielectric material. This technique has been under development for more than a decade. The task of image reconstruction for ECT is to determine the permittivity distribution and hence material distribution over the cross-section from capacitance measurements. There are three principal difficulties with image reconstruction for ECT: (1) the relationship between the permittivity distribution and capacitance is non-linear and the electric field is distorted by the material present, the so-called ‘soft-field’ effect; (2) the number of independent measurements is limited, leading to an under-determined problem and (3) the inverse problem is ill posed and ill conditioned, making the solution sensitive to measurement errors and noise. Regularization methods are needed to treat this ill-posedness. This paper reviews existing image reconstruction algorithms for ECT, including linear back-projection, singular value decomposition, Tikhonov regularization, Newton–Raphson, iterative Tikhonov, the steepest descent method, Landweber iteration, the conjugate gradient method, algebraic reconstruction techniques, simultaneous iterative reconstruction techniques and model-based reconstruction. Some of these algorithms are examined by simulation and experiment for typical permittivity distributions. Future developments in image reconstruction for ECT are discussed.

2.2 “Sensitivity Matrix Calculation for Fast 3-D Electrical Capacitance Tomography (ECT) of Flow Systems”,[2]

In this paper, we discuss an improved three-dimensional (3-D) sensitivity matrix calculation and measurement approach for ECT of flow systems

employing neural-network (NN)-based inverse algorithms. The numerical calculation is based on a hybridization of finite-element method (FEM) solution and perturbative techniques for different discretization regimes (pixel sizes) and pixel locations. The experimental apparatus involved, the sensor design, and inverse techniques are also discussed. Simulation results of the imaging of flows systems are provided to illustrate the capabilities of the ECT technique for 3-D imaging of flow systems.

2.3 “Tomographic imaging of industrial process equipment: techniques and applications”,[3]

Opportunities for the use of noninvasive tomographic sensor technology are described and reviewed critically. Imaging instruments based on electrical sensing methods are discussed with respect to a number of process applications, including measurement of component concentration profiles, phase boundaries, component velocities and component mass flow rate. The use of low-noise electronic devices for process image sensing and the computationally intensive digital signal processing systems for image reconstruction are discussed. Limitations of current electronic techniques, particularly for future ultra high speed image reconstruction are revealed and directions for future progress are elucidated.

2.4 “New Progress of the Digital Electrical Capacitance Tomography System for Gas/Liquid Two Phase Flow”,[4]

Electrical capacitance tomography (ECT) is gaining acceptance as a laboratory and industry tool to analyze gas/liquid two phase flow. To overcome the shortcomings of the existing analogue ECT system, a new 16-electrode digital electrical capacitance tomography system based on FPGA and DSP is designed. The new scheme can easily realize single frequency and multi-frequency excitation and demodulation. Furthermore, two kinds of methods for multi-frequency demodulation, DFT demodulation and digital quadrature demodulation, are discussed deeply. Static and dynamic experiments under condition of single frequency are carried out to verify the performance of the digital ECT system. Experimental results show that this system is of high precision and stability.

2.5 “Electrical impedance imaging system using FPGAs for flexibility and interoperability”,[5]

Modern EIT systems require simultaneously operating multiple functions for flexibility, interoperability, and clinical applicability. To implement versatile functions, expandable design and implementation tools are needed. On the other hand, it is necessary to develop an ASIC-based EIT system to maximize its performance. Since the ASIC design is expensive and unchangeable, we can use FPGAs as a prior step to the digital ASIC design and carefully classify which functions should be included in the ASIC. In this paper, we describe the details of the FPGA design adopted in the KHU Mark2.5 EIT system.

2.6 “A Digital Switching Demodulator for Electrical Capacitance Tomography”[6]

In this paper, a digital switching demodulator is presented for use in ac-based electrical capacitance tomography systems. Implementing a switching phase-sensitive demodulator (PSD) digitally offers the following advantages: 1) Demodulation can be implemented using a programmable digital device, and hence, CMOS switches, which are used in a conventional switching PSD, are no longer needed; 2) compared with the widely used digital quadrature PSD, this proposed demodulator is simple in configuration because neither a reference signal nor multiplication is required; 3) according to the specific requirements, the new demodulator can be implemented in two operation modes, i.e., the amplitude mode and the phase-sensitive mode; and 4) because only subtractions and accumulations are needed, the proposed demodulator can be easily implemented with low-cost logic devices, e.g., a complex programmable logic device (CPLD). By simulation, the feasibility and effectiveness of the proposed demodulator have been confirmed. CPLD-based and field-programmable gate-array-based capacitance measurement circuits are constructed, and the performances of different demodulation methods are compared. Both simulation and experiment show that the proposed demodulator can provide demodulation results with high signal-to-noise ratio. The system design can be simplified using the digital switching demodulator.

2.7 “Hardware Acceleration of Iterative Image Reconstruction for X-Ray Computed Tomography”,[7]

X-ray computed tomography (CT) images could be improved using iterative image reconstruction if the 3D conebeam forward- and back-projection computations can be accelerated significantly. We investigated the feasibility of a field-programmable gate array (FPGA) implementation of the separable footprint (SF) forward projector. A 16-bit fixed-point quantization introduces negligible numerical errors without affecting the perceptual image quality. The SF-based 3D cone-beam projector can be efficiently parallelized and its memory bandwidth reduced by exploiting projection geometry and data locality. We demonstrate a fully pipelined, 75-way parallel hardware architecture of the SF forward projector on a Xilinx Virtex-5 FPGA that can complete one forward projection of a $320 \times 320 \times 61$ object over 3,625 views in 6.3 seconds.

2.8 “NoC-Based FPGA Acceleration for Monte Carlo Simulations with Applications to SPECT Imaging”,[8]

As the number of transistors that are integrated onto a silicon die continues to increase, the compute power is becoming a commodity. This has enabled a whole host of new applications that rely on high-throughput computations. Recently, the need for faster and cost-effective applications in form-factor constrained environments has driven an interest in on-chip acceleration of algorithms based on Monte Carlo simulations. Though Field Programmable Gate Arrays (FPGAs), with hundreds of on-chip arithmetic units, show significant promise for accelerating these embarrassingly parallel simulations, a challenge exists in sharing access to simulation data among many concurrent experiments. This paper presents a compute architecture for accelerating Monte Carlo simulations based on the Network-on-Chip (NOC) paradigm for on-chip communication. We demonstrate through the complete implementation of a Monte Carlo-based image reconstruction algorithm for Single-Photon Emission Computed Tomography (SPECT) imaging that this complex problem can be accelerated by two orders of magnitude on even a modestly sized FPGA over a 2 GHz Intel Core 2 Duo

Processor. The architecture and the methodology that we present in this paper is modular and hence it is scalable to problem instances of different sizes, with application to other domains that rely on Monte Carlo simulations.

2.9 “Parallelization of Tau-Leap Coarse-Grained Monte Carlo Simulations on GPUs”,[9]

The Coarse-Grained Monte Carlo (CGMC) method is a multi-scale stochastic mathematical and simulation framework for spatially distributed systems. CGMC simulations are important tools for studying phenomena such as catalysis, crystal growth, surface diffusion, phase transitions on single crystals, and cell membrane receptor dynamics. In parallel CGMC, the tau-leap method is used for parallel simulations that are executed on traditional CPU clusters in a master-slave setting. Unfortunately the communications between master and slaves negatively impact speedup and scalability. In this paper, we explore the potentials of GPUs for the tau-leap method and we present an extensive performance evaluation that leads to the most suitable degree of parallelism for this method under different simulation profiles. We show how the efficient parallelization of the tau-leap method for GPUs includes (1) the redefinition of its data structures, (2) the redesign of its algorithm, and (3) the selection of the most appropriate degree of parallelism (i.e., fine-grained or coarse-grained) on a single GPU or multiple GPUs. Exceptional performance improvements can thus be achieved for this method.

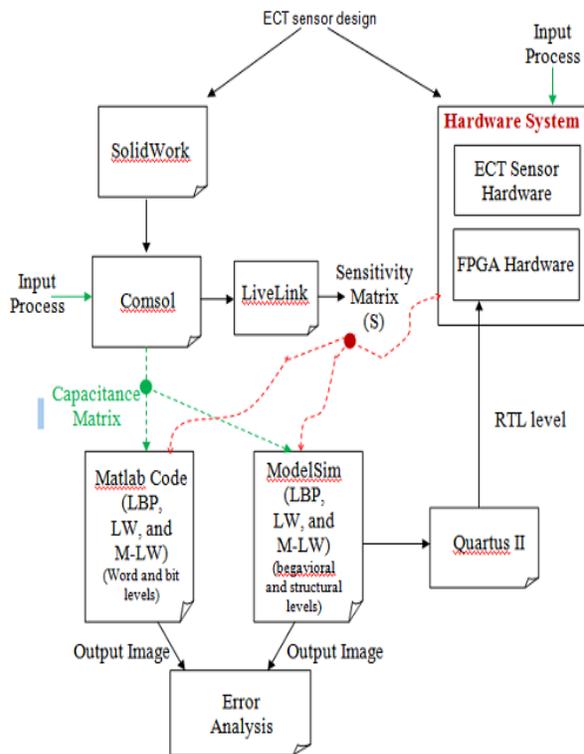
2.10 “Fully Digital FPGA-Based Data Acquisition System for Dual Head PET Detectors”,[10]

We present the development of a new fully digital, flexible, cost-efficient data acquisition system (DAQ) suitable for dual head Positron Emission Tomography (PET) scanners for small animal imaging applications. A free-running 12 bit octal channel Analog to Digital Converter (ADC), with 65 MHz sampling rate, was used for the digitization of the detector signals. The digitized data were fed into a Spartan 6 Field Programmable Gate Array (FPGA) for event processing. An embedded system was developed for the acquisition, using Xilinx’s Embedded Development Kit (EDK) and Microblaze processor. A digital version of the Constant Fraction

Discriminator (CFD) method was implemented in the FPGA, in order to achieve higher time resolution than the ADC sampling period, eliminating the need of an external mixed-signal device. The obtained information using FPGA includes: event timing, energy determination-discrimination, position determination and coincidence processing. The online processing of potential coincident events, significantly reduces the amount of data that will be transmitted to the computer. Coincident events are written temporarily to an external memory provided on a development board and are transferred to a Personal Computer (PC), via Ethernet link, for image reconstruction. Minimal post processing of the data is required prior to reconstruction. A small detector pair consisting of a BGO array coupled to a Position Sensitive Photomultiplier Tube (PSPMT) was used for the evaluation of the readout system. Obtained results prove that the proposed architecture can be used for the readout of dual head PET detectors for small animal imaging applications.

III METHOD AND ANALYSIS

The design flow used various commercially-available software tools, namely SolidWork, Comsol, Livelink, and Matlab for high level simulation and Modelsim and Quartus II for hardware level simulation.



Overview of the Hardware/Software Codesign Methodology

IV CONCLUSION

The hardware explored the implicit parallelism for matrix multiplication. Its advantage is that it is flexible to accommodate various bit-widths and image sizes, in addition to consume less power since the most significant bits of the sensitivity matrix are usually equal zero. In order to achieve 1 pixel per clock cycle throughput, a new pipelined architecture was suggested. Extensive simulations indicate that the proposed architecture achieves a speed-up of up to three orders of magnitude over the software version when the reconstruction algorithm runs on 2.53 GHZ-based Pentium processor. This satisfies the real-time constraint of many industrial applications. To the best of the authors' knowledge, this is the first embedded system which explores the intrinsic parallelism which is available in modern FPGA for ECT tomography.

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