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Realization of modified low power and area efficient reconfigurable fir filter

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ABSTRACT

The project presents design of low power and area efficient FIR filter using LMS (Least Mean Square) Algorithm. Least Mean Squares algorithm used in many DSP applications to process the signal and designed for generating filter coefficients based on the processed signal. The proposed method reduces the power consumption and area due to adaptation of the weights generated internally according to the corrected output and previous weights. The weights area calculated using LMS algorithm. The variable filter is an FIR filter due to its stability, which has larger amplitude variations in input data and filter coefficients. As filtering part is the major contributor of power in an adaptive system, cancellation of multiplication will cause a significant.

Keywords: LMS (Least Mean Square) Algorithm, DSP applications, FIR filter due to its stability.

INTRODUCTION

Filters are a basic component of all signal processing and telecommunication systems. Filters are widely employed in signal processing and communication systems in applications such as channel equalization, noise reduction, radar, audio processing, video processing, biomedical signal processing, and analysis of economic and financial data. For example in a radio receiver band-pass filters, or tuners, are used to extract the signals from a radio channel. Finite impulse response (FIR) filters are the most popular type of filters implemented in software. A digital filter takes a digital input, gives a digital output, and consists of digital components. In a typical digital filtering application, software running on a digital signal processor (DSP) reads input Samples from an A/D converter, performs the Mathematical manipulations dictated by theory for the required filter type, and outputs the result via a D/A converter. An analog filter, by contrast, operates directly on the analog inputs and is built entirely with analog components, such as resistors, capacitors, and inductors. Digital signal processing applications are common in home entertainment systems, television sets, high-fidelity audio equipment, and information systems. The digital filter is an important component in mathematical operations on a sampled, discrete-time signal to enhance the certainty of a signal. The digital filter is characterized by its transfer function. Two digital filters are infinite impulse response (IIR) and finite impulse response (FIR) filters [1-10].

LITERATURE SURVEY

Marcos Martínez-Peiró, Eduardo Boemo and Lars Wanhammar (2002). “Design of High-Speed Multiplier less Filters Using a Non recursive Signed Common Sub expression Algorithm” In this work, a new algorithm called non recursive signed common sub expression elimination (NR-SCSE) is discussed, and several applications in the area of multiplier less finite-impulse response (FIR) filters are developed. While the recursive utilization of a common sub expression generates a high logic depth into the digital structure, the NR-SCSE algorithm allows the designer to overcome this

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problem by using each sub expression once. The paper presents a complete description of the algorithm, and a comparison with two other well-known options: the graph synthesis, and the classical common sub expression elimination technique.

Kenny Johansson, Oscar Gustafson, and Lars Wanhammar (2007). "Bit-Level Optimization of Shift-and-Add Based FIR Filters" Implementation of FIR filters using shift-and-add multipliers has been an active research area for the last decade. However, almost all algorithms so far has been focused on reducing the number of adders and subtractors, while little effort was put on the bit-level implementation. In this work we propose a method to optimize the number of full adders and half adders required to realize a given number of additions. We present results which show that both area and power consumption can be reduced using the proposed method.

Mathias Faust and Chip-Hong Chang (2009). "Optimization of structural adders in fixed coefficient transposed direct form FIR filters" In this paper, an optimization method for the structural adders in the transposed tapped delay line is proposed. Although additional registers are required, an optimal trade-off can be made such that the overall combinational logic is reduced. For a majority of taps, the delay through the structural adder is shortened except for the last tap. The one full adder delay increase for the last optimized tap is tolerable as it does not fall in the critical path in most cases. The criterion for which area reduction is possible is analytically derived and an area reduction of up to 4.5% for the structural adder block of three benchmark filters is estimated theoretically. The saving is more prominent as the number of taps grows. Actual synthesis results obtained by Synopsys Design compiler with 0.18µm TSMC CMOS libraries show a total area reduction. designed using cse and gd.This filter using coefficient mapping method [11-12].

PROPOSED SYSTEM

Lms Adaptive Filter

They have proposed a fine-grained pipelined design to limit the critical path to the maximum of one addition time, which supports high sampling frequency, but involves a lot of area overhead for pipelining and higher power consumption due to large number of pipeline latches. An efficient adder tree for pipelined inner-product computation is used to minimize the critical path and silicon area without increasing the number of adaptation delays.

An efficient architecture is used for the implementation of a delayed LMS adaptive filter. We also find that the proposed design offers less area, less energy than the best of the existing systolic structures, on average, for filter lengths N = 8.The proposed structure for the weight-update block is shown in below. It performs N multiply-accumulate operations of the form (µ × e) × xi + wi to update N filter weights for each condition.

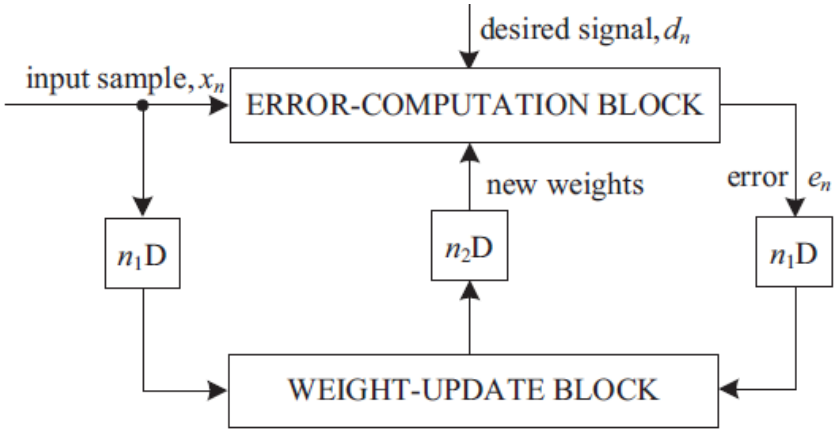

Figure Proposed Modified LMS Adaptive Filter

(Least Mean Square) LMS algorithm

Most widely use algorithm in adaptive filter is an LMS algorithm due to its simplicity. It doesn't needs an extra mathematical calculation like matrix inversion nor is correlation function .Mean Square Error (MSE) logic used in LMS algorithm. It uses an input signal, step-size parameter, the subtraction

of desired signal and filter output signal for calculating the updated filter coefficients

LMS Equation

Based on the filter taps and input response the equation will be obtained for number of iterations. The equation to updated tap weight w (n) using the input signal x (n) and the desired response d (n) with step size μ is shown in equation:

$$\mathbf{w(n+1) = w(n) + \mu x(n)[\, d(n) - x(n)w(n)]}$$

Whereas μ is the step size, hence the filter output is the sum of the product of tap weights and input signal

$$y(n) = x(n) * w(n) \quad (2)$$

Error signal e (n) is defined as the subtraction of the desired signal and the filter response signal

$$e(n) = d(n) - y(n) \quad (3)$$

So, Equation (1) can be further written in terms of the error signal and the tap weights:

$$w(n+1) = w(n) + \mu x(n)\, e(n) \quad (4)$$

Fir Filter Design Using Lms

To implement the LMS algorithm, during each sampling period of training phase, one has to compute a filter output and an error value which equals to the difference between the current filter output and the desired response. The estimated error is used to update the filter weights in every cycle. In case of pipelined designs, the Feedback error (n) corresponding to the nth iteration is not available for updating the filter weights in the same iteration. It becomes available after certain number of cycles, called the adaptation delays. The DLMS algorithm therefore uses the delayed error. In this method the critical path is reduced by using a pipelined register structure.

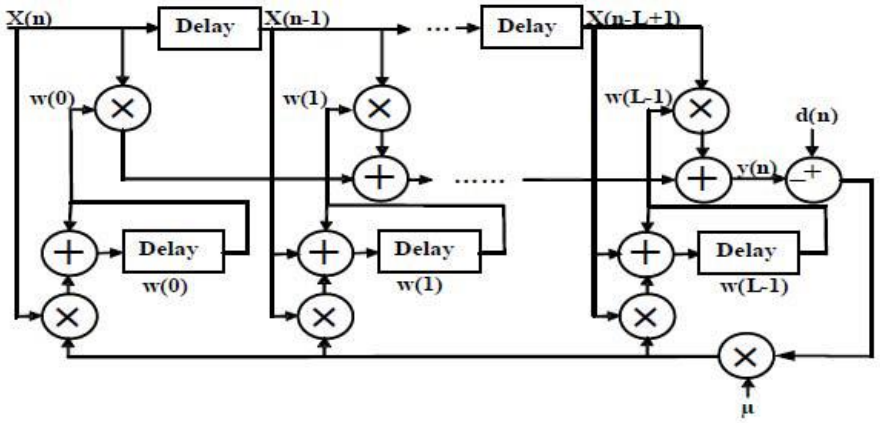

Figure Structural view of FIR filter with weights using LMS algorithm

SOFTWARE DESCRIPTION

Very-Large-Scale Integration (VLSI)

Very-large-scale integration (VLSI) is the process of creating integrated circuits by combining thousands of transistors into a single chip. VLSI began in the 1970s when complex semiconductor and communication technologies were being developed. The microprocessor is a VLSI device. The term is no longer as common as it once was, as chips have increased in complexity into billions of transistors

VHDL (VHSIC Hardware Description Language)

Used in electronic design automation to describe digital and mixed-signal systems such as field-programmable gate arrays and integrated circuits.

Architecture

The most common FPGA architecture [26] consists of an array of logic blocks (called Configurable Logic Block, CLB, or Logic Array Block, LAB, depending on vendor), I/O pads, and routing channels. Generally, all the routing channels have the same width (number of wires). Multiple I/O pads may fit into the height of one row or the width of one column in the array. ALMs and Slices usually Contains 2 or 4 structures similar to the example figure, with some shared signals.

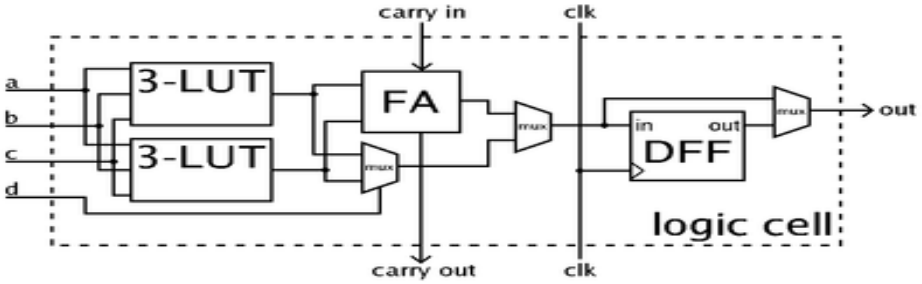

Figure Simplified example illustration of a logic cell

RESULTS AND DISCUSSION

Perfomance Results

This section evaluates the performance of the proposed modified least mean square (LMS) algorithm and shows the simulation results. The first result declares about the output of LMS adaptive filter with delay. It is having some delay in the output of Least Mean Square adaptive filter. And the second result declares about the output of LMS adaptive filter without delay.

Simulation Test

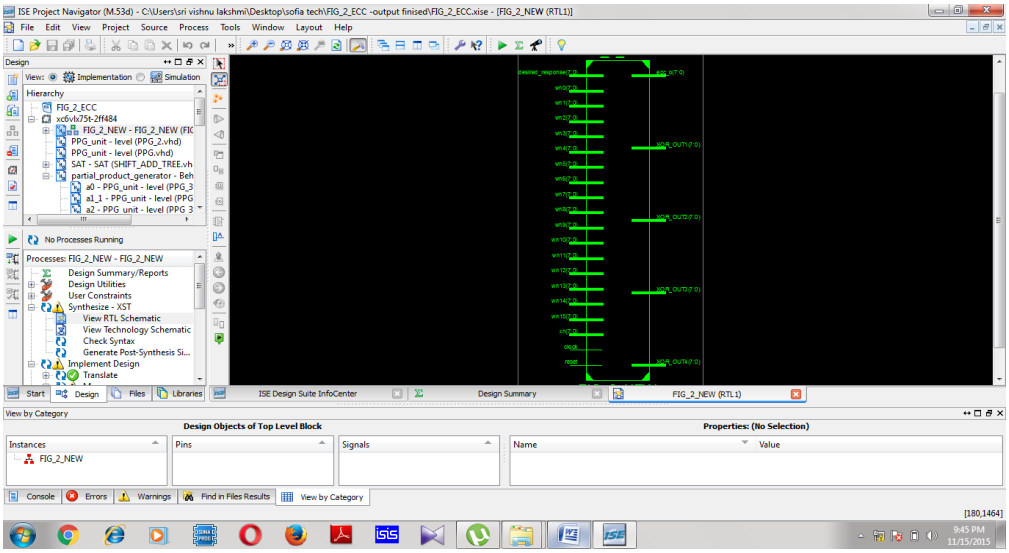

Figure: LMS Adaptive Filter

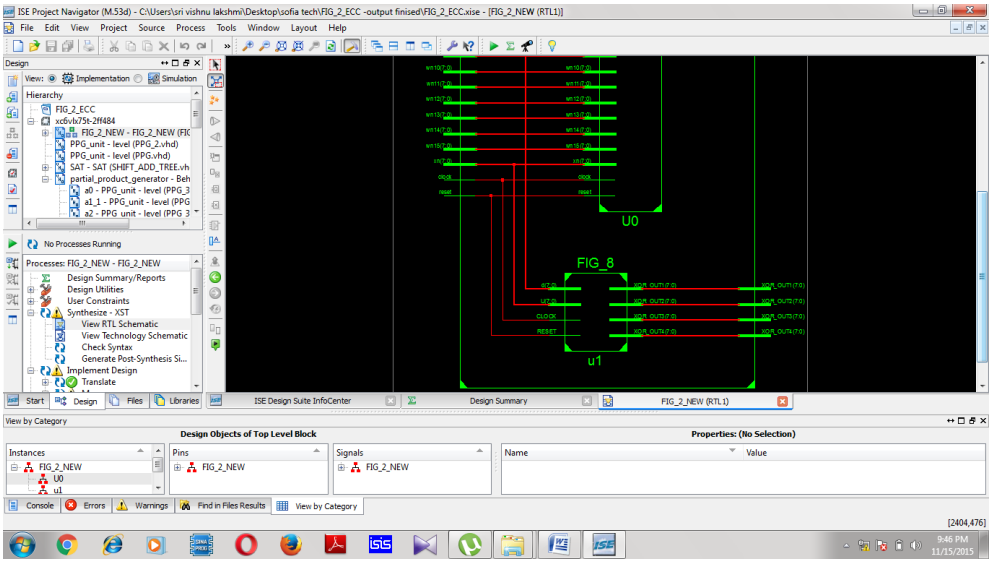

Figure: Proposed System RTL Diagram

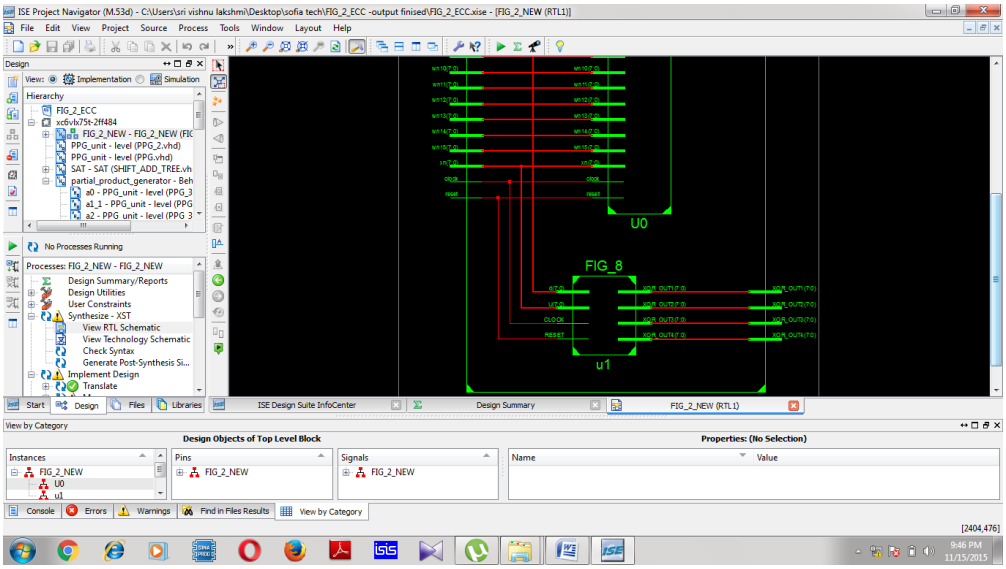

Figure: Proposed RTL Technology Diagram

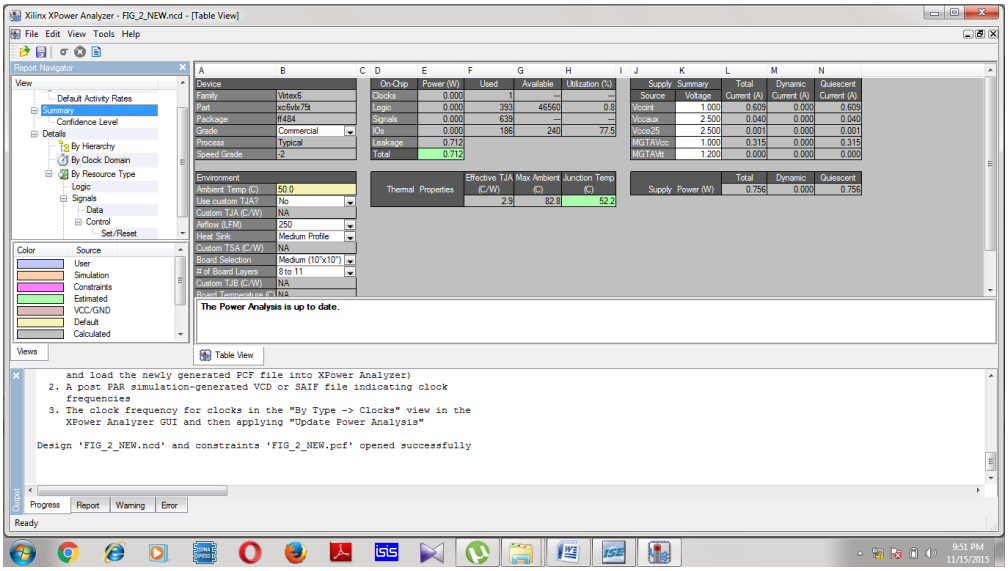

Figure: Power Analyzer Output

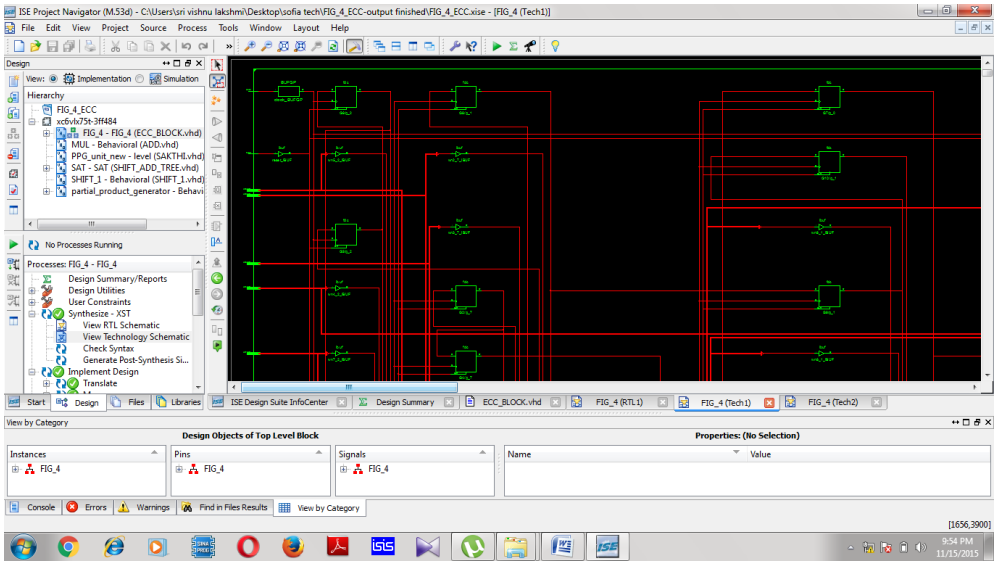

Figure: Error Computation Block RTL Diagram

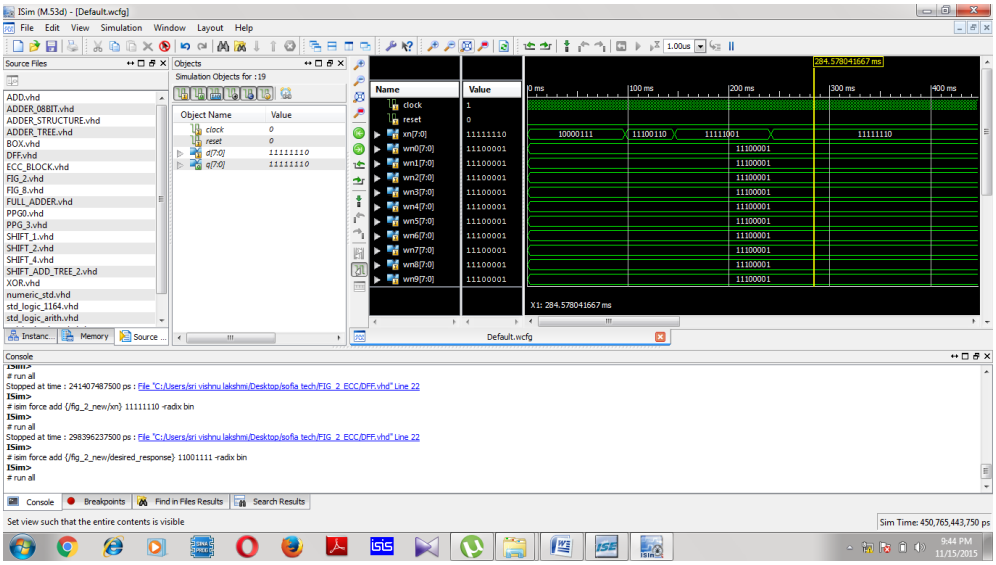

Figure: Fir Filter Using LMS Output

CONCLUSION

In this project, low power architecture for adaptive filter is proposed. The low power adaptive filter consists of a reconfigurable low power FIR filter and the LMS algorithm. The LMS algorithm is used to update weights of reconfigurable filter with low complexity. The experimental results showed significant reduction in power. The application of low power adaptive filter to noise cancellation is demonstrated using a signal with injected noise. The proposed low power adaptive filtering system can also be used for other applications such as system identification, echo cancellation etc. We proposed a strategy for optimized balanced pipelining across the time-consuming blocks of the structure to reduce the adaptation delay and power consumption. The highest sampling rate that could be supported by the ASIC implementation of the proposed design ranged from about 875 to 1015 MHz for filter orders 9 to 35. The adaptive filter is required to be operated at a lower sampling rate, with a clock slower than the maximum usable frequency and a lower operating voltage to reduce the power consumption The efficient addition scheme reduces the adaptation delay to achieve the faster performance and reduction in the critical path supports the high input-sampling rates

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