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Design and analysis of area efficient, high speed PLL using 90nm CMOS technology

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ABSTRACT

Speed and Area are the important parameters in various designing systems. Low power design is essential to extend the operating time of integrated circuits (ICs) additionally on reduce the packaging and cooling costs. The Phase locked loop (PLL) is an efficient method employed in frequency synthesis. Because the scale of integration keeps growing, VLSI chip is employed to implement the signal processing systems, which was more and more complex. These signal processing applications consume impressive amount of energy. The tradeoff between performance and area remain to be the two major design factors, high power consumption is critical in today's VLSI system design. In this paper CMOS VLSI dynamic logic is employed to induce high speed, less area and reduced power of the PLL system. A dynamic logic based CMOS is proposed to design the phase detector, Voltage Controlled Oscillator and loop low pass filter (LPF). The CMOS dynamic logic is the High speed logic in all the CMOS logic families. The DSCH3 tool is employed in the design of logical circuits and micro wind 3.1 tool using 90nm CMOS technology is employed to measure the parametric analysis. The bandwidth of loop filter is the speed of the transition time between synthesized frequencies. In the dynamic CMOS logic PLL, the speed is improved to 7.25GHZ and area is reduced to 204.2 μm².

Keyword: PLL, CMOS Dynamic logic, VCO, LPF, Microwave, RF.

INTRODUCTION

Phase Locked Loop

A phase locked loop (PLL) is known as a control system that generates associate phase signal which is related to the phase signal of an input. The Simplest form in some of the different types is an electronic circuit design consisting of a changeable frequency oscillator and also a phase detector in the loop, which is given as feedback. The oscillator generates a signaling, and therefore the phase detectors compare the phase of the signal with the phase of the input periodic signal and also adjust the oscillator to hold the phases matched.

Maintaining the frequencies of input and output as identical means holding the input and output phases in lock. Therefore, in additional to synchronizing signals, a phase locked loop can multiple the input frequency and generate a series frequencies, or the input frequency can be tracked. There are several variations of PLLs. Some of them are analog phase locked loop (APLL) also said as a linear phase locked loop (LPLL), digital phase locked loop (DPLL), all digital phase locked loop (AD-PLL), and software phase locked loop (SPLL).In APLL ,Phase detector is an analog multiplier and Loop filter is active or passive and also uses a voltage-controlled oscillator (VCO). APLL is alleged to be a type II if its loop filter has transfer function with exactly one pole at the origin. An Analog PLL along with a digital phase detector is known as the DPLL. For instance, a

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PLL with XOR phase detector or edge triggered phase detector or else phase frequency detector. In ADPLL May have digital divider within the loop. Phase detector, filter and oscillator are digital. Uses a numerically controlled oscillator (NCO). In SPLL Functional blocks are implemented by software instead of specialized hardware. In DPLL it replaces process and noise-sensitive analog circuits with digital equivalents. Increases PLL design portability and testability, takes advantage of area scaling with nm devices, it's greater flexibility in loop bandwidth so low capacitors is enough to provide low band width, increases ability to check and observe, Fast behavioural simulation, Good-enough for frequency synthesis applications.

Phase detector

A phase detector (PD) represented generates a voltage, which represents the phase difference between two signals. In a PLL, the 2 inputs of the phase detector are the reference input and also the feedback from the VCO. The PD output voltage is employed to regulate the VCO so that the phase difference between the 2 inputs is held constant, making it a feedback system that is negative. There are various types of phase detectors each have their identical performance characteristics. The double balanced mixer or diode ring mixer is one amongst the best types of phase detector. The double balanced mixer of diode ring phase detector could be a simple and effective kind of phase detector which can be implemented employing a standard diode ring module. The exclusive OR, XOR phase detector circuit can provide a really useful simple phase detector for a few applications. It comprises of a logically exclusive OR circuit. Being digital in format it can often fit into a phase locked loop with ease as many of the circuits related to the phase locked loop may already be in an exceedingly digital format. Alternatively, an exclusive OR can be made up of discrete components to relinquish a wider sort of levels and other options. The XOR edge triggered phase detector is generally used because it is independent of the duty cycle and therefore the frequency correction is taken into account more importantly over phase correction [1-5].

The frequency blender produces harmonics that adds difficulty in applications where spectral clarity of the VCO signal is very essential. The resulting unessential (spurious) side bands, also known as "reference spurs" can stand over the filter requirements and decrease the capture range well below or expand the lock time beyond the requirements. In these applications the more problematical digital phase detectors are employed which do not have as extreme reference spur component on their output. Consequently, when in lock, the steady-state phase difference at the inputs using this sort of phase detector is near 90 degrees.

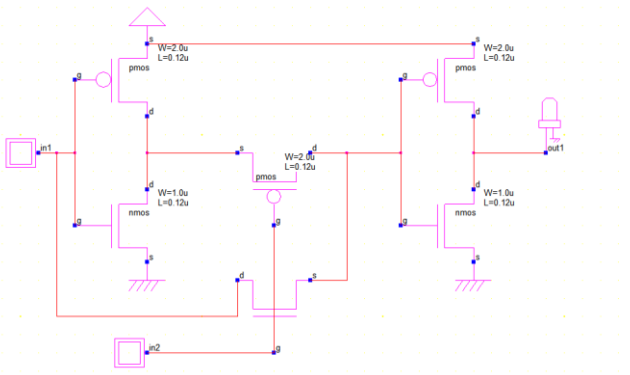

Figure.1.1. Schematic design of phase detector.

Low Pass Filter

The PLL loop filter (usually a low pass loop filter) generally has two distinct functions. The foremost function is to work out loop dynamics, also called stability. This can be how the loop responds to interferences, such as the changes within the reference frequency, the changes of the

feedback divider, or the changes at the start up. Common considerations are the range over which the loop are able to do lock (pull-in range, lock range or capture range), how briskly the loop achieves lock (lock time, lock-up time or settling time) and damping behaviour. Reckoning on the application, this might require one or more of the following: an easy proportion (gain or attenuation), an integral (low pass filter) and/or derivative (high pass filter) [6-10].

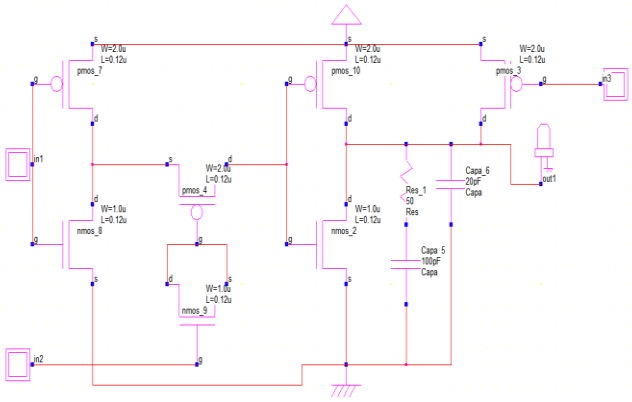

Figure.1.2. Schematic design of LPF

Loop's gain margin and phase margin are the most commonly examined loop parameters. Common concepts in control theory including the PID controller are accustomed to design this function .The following common consideration is controlling the quantity of reference frequency energy (ripple) surfacing at the phase detector output that is after it is applied to the VCO control input. This frequency regulates the VCO and produces FM side bands commonly called "reference spurs". The filter should be as close-packed as possible. The oscillation frequency of the VCO is proportional to the output voltage of the loop filter controls.

Voltage Controlled Oscillator

All phase locked loops utilize an oscillator element with changeable frequency capability. This could be an analog VCO either driven by analog circuitry in the case of an APLL or driven digitally through the utilization of a digital-to-analog converter as is that the case for a few DPLL designs. The AD PLLs employ only Pure digital oscillators such as a numerically controlled oscillator. PLLs may include a divider between the oscillator and therefore the feedback input to the phase detector to develop a frequency synthesizer.

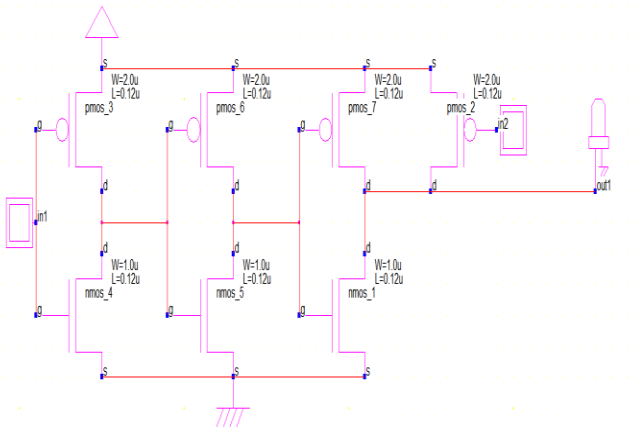

Figure.1.3. Schematic design of VCO

It should even be noted that the feedback is not limited to a frequency divider. This element may be other elements such as a frequency multiplier, or a mixer. The VCO output is made to a sub multiple (rather than a multiple) of the reference frequency by the multiplier. A mixer can translate the VCO frequency by a unchangeable offset. It is going to even be a combination of those. An example being a divider following a mixer; this permits the divider to control at a way much lower frequency than the VCO without a loss in the loop gain.

SYSTEM DESIGN

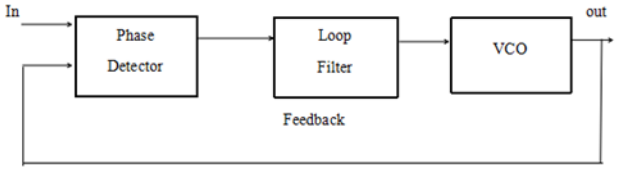

Figure.2.1.Block diagram

The basic functional block diagram of PLL is shown in Figure.3.1. The output frequency and the input frequency are continuously monitored and the number of replicating repetitions will reduce the phase difference. It consists of three blocks namely,

- Phase detector
- Low pass filter
- Voltage controlled oscillator

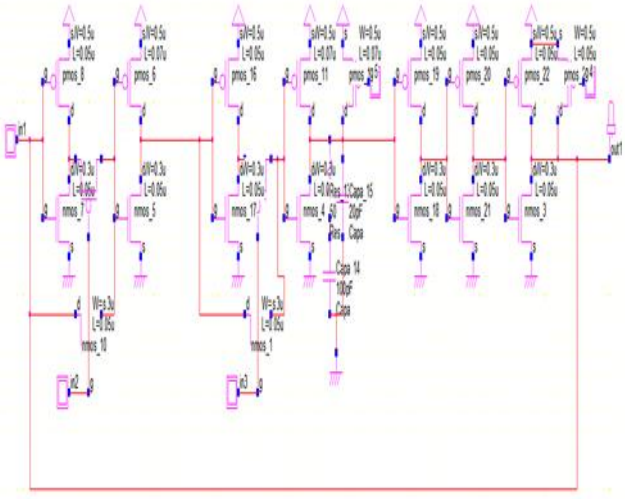

Figure.2.2. Schematic design of PLL

For development of digital phase detector, a XOR logic gate is employed. The XOR gate is designed by using various logic gates i.e., AND & OR gate. In this phase detector design, used XOR implementation using CMOS dynamic logic. The quantity of transistors is reduced in XOR logic. In order to attain high speed of operation with less power, CMOS dynamic logic has been chosen. When the phase of input and output signals is same then the XOR gate's output is going to be logic zero. When the phase of input and output signals are not seem to be same, the output is going to be logic one.

Using CMOS dynamic logic, the loop filter is designed. It allows only the low frequencies and attenuate high frequencies by the loop low pass

filter and thus noise is removed. The phases between the PLL output signal voltage and the input reference signal voltage are continuously compared. The phase difference between them is proportional to the loop filter output signal. It offers an enable signal to the oscillator. To pick out a specific band of frequency, frequency selective circuits are used whereas the overall noise in phase will be suppressed by VCO control line input.

Voltage-Controlled Oscillator (VCO) is designed in the CMOS dynamic logic. A Voltage Controlled Oscillator (VCO) is an electronic circuit whose oscillation frequency is controlled by an input signal voltage. The applied input voltage regulates the instantaneous oscillation frequency. It is very challenging to design VCO which has high frequency deviation, Adequate VCO sensitivity, good phase stability and capability of accommodating wide band modulating signal.

LAYOUT DESIGN

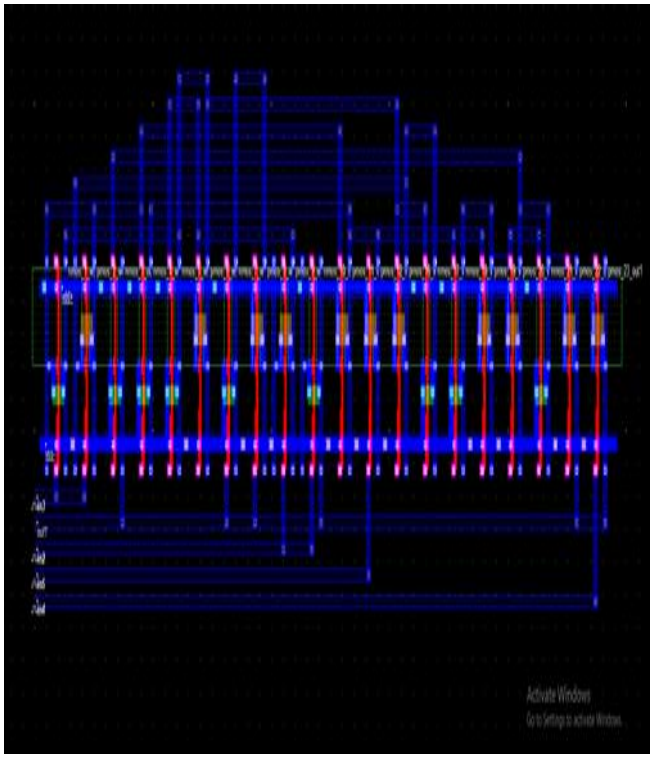

Figure.3.1. Layout design of phase locked loop

The Layout Diagram of PLL is shown in Figure.3.1. After the design of PLL by cascading the three blocks, make the Verilog file of the schematic circuit designed in the DSCH3 software tool. Then the layout design of PLL is obtained by compiling the Verilog file in the Micro wind software.

PROCEDURE

Schematic design or transistor level design is designed using DSCH3 tool

- All three blocks of PLL are designed and connected to form PLL
- This is then converted into layout design using microwind2 tool
- Verified for DRC and then simulated
- Finally, parametric analysis is done for various parameters

RESULTS

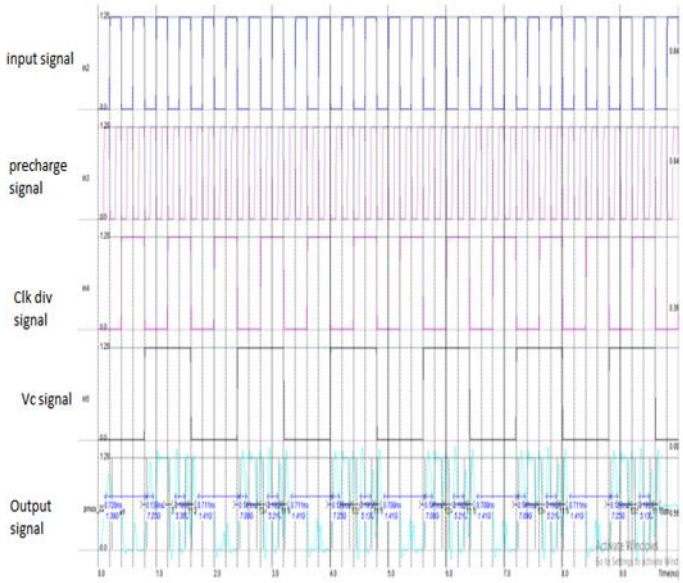

Figure.5.1. Simulated output for PLL

The Simulated output of layout design for PLL is shown in Figure.5.1. micro wind tool is used to check the design rule for the layout design simulated and then the waveform is simulated. The parametric analysis is done using micro wind tool.

Table.5.1. Parametric analysis

Parameters	Results
Area	204.2μm²
Speed	7.25GHz
Power	0.630mW
Time Delay	0.133ns
height	8.2μm
width	24.9μm

CONCLUSION

It is seen that using dynamic CMOS technology, many parameters like speed, area, power, etc can be optimized with respect to advancing techniques. Time delay, height and width of each and every transistor are also seen within the parametric analysis. The proposed dynamic CMOS Phase Locked Loop can operate at very high speed in which the speed is improved up to 7.25GHz with less power consumption of 0.630mW. In the design the number of transistors is reduced using 90 nm technology thus reducing the area to 24.9x8.2 μm. The proposed PLL generate a range of frequencies from 3.83 GHz to 7.25 GHz. The desired range of frequencies is super high frequency range that can be employed in variety of industries. The proposed PLL is most suitable for microwave antennas. In microwave antennas, for point-to-point connection this range of frequencies is used. This is often helpful in transferring audio, video signals and messages. It can also be implemented in communication applications such as frequency synthesis for missile tracking and also in Radio Frequency (RF) and microwave synthesizer. The height and width of the transistor can be changed or reduced in order that many transistors can be placed and using

various VLSI technologies, the parameters like area, power can be improved. Power reduction can be done by reducing the number or quantity of transistors furthers more. The evolution in frequency generation involving various innovations in process, circuit, and packaging technologies provides with greater functionality and performance in a smaller form factor than previous discrete solutions. Ultimatum for spectral clarity has driven innovations in filtering ICs that pair with these newly developed synthesizer ICs providing low phase noise, highly spectrally pure millimeter wave signal sources for the request of modern wireless applications. The flexibleness and simplicity enabled by the wideband PLLs/VCOs greatly shorten design time. The phase-noise improvement, super-fast lock times, and ability to adapt the incoherent within the architecture are likely to dominate Local Oscillator blocks of future multi-standard high-data-rate wireless systems and most recently, the 5G Communication standards. In RF Employing a frequency synthesizer to set the frequency rather than the potentiometer increase the accuracy.

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