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Fuzzy logic based comparative circuit topology for unified power quality conditioner without degrading the performance

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ABSTRACT

This paper proposes a new topological configuration for a unified power quality conditioner (UPQC). Generally, the power structure of three-phase-three-wire UPQC consists of two back-to-back connected six switch inverters. For this configuration, out of twelve switches, six of the series inverter switches will be under-utilized most of the time. To improve the semiconductor utilization and consequently to reduce the total switch count, this paper proposes a new reduced switch topology for UPQC. The proposed topology is realized using only ten switches and retains all the performance merits of the twelve-switch UPQC while minimizing its underutilization without increasing the switch VA rating. The paper provides a detailed analytical study and evaluation by comparing the proposed topology with the twelve and nine switches based UPQC system configurations. The feasibility of the proposed topology is validated through experimental investigation

Keywords: Dtmf, Pic Controller, Gsm Modem

INTRODUCTION

The ever increasing use of solid state technology in industrial and domestic applications is extensively contributing towards line current harmonics, leading to non-linear voltage drops, cables overheating, poor power factor and additional power losses at distribution levels . To mitigate these problems and maintain the reliability of the delivered power within acceptable margins, stringent power quality standards are put into practics. The adherence to these standards can be achieved with a custom power device such as the unified power quality conditioner (UPQC) . Being a versatile and flexible power (VSI), connected in shunt and series configuration with the grid, at the point of common coupling (PCC) and share a common dc link capacitor . The series VSI protects the downstream loads from sags/swells in the PCC voltage whereas the shunt VSI reduces the upstream line losses by compensating the harmonic distortion and reactive component of the load current. When the voltage at PCC is distorted, the series VSI can be additionally controlled to mitigate and prevent the voltage harmonics from reaching the load . There is an extensive literature available on UPQC and a detailed review can be found in Although back-to-back UPQC with twelve switches offers independent control of both VSIs and excellent mitigation of grid disturbances, its series VSI is generally underutilized. During normal conditions the series VSI (six out of twelve switches) remain either completely inactive or operate at very low modulation index. This under-utilization of the series VSI may give rise to computational problems as addressed in.

This paper proposes a new reduced switch UPQC system topology that comprises of ten switches in total. The main objective is to reduce the overall switch count of the back-to-back UPQC system while retaining its operational features without any performance tradeoff. To maintain the linear modulation range and uniform switching frequency for all the switches within the proposed topology, a carrier based double zero sequence injection scheme is also developed. An appropriate

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control algorithm is developed to achieve the seamless operation of the proposed UPQC topology under different operating conditions. An experimental study is carried out to validate the performance of the proposed topology.

THREE PHASE THREE WIRE UPQC SYSTEM CONFIGURATIONS

For three-phase-three-wire system, generally, the back-to-back inverter based UPQC system is widely used and is shown in Fig. 1. It comprises of twelve power semiconductor switches in total. Switches { constitute the shunt VSI which is connected at the PCC, whereas, the switches constitute the series VSI and is connected between the PCC and load. Both inverters share the common dc link capacitor. As shown in Fig. 1, the twelve-switch UPQC deploys two dedicated inverters for performing the UPQC functionalities.

Fig. 1. Twelve-switch UPQC topology.

This feature allows UPQC to have shunt VSI connected at either the PCC or load with no effect on the compensation ability.

Recently, there has been an effort to reduce the total switch count of the UPQC as reported in By merging the lower three switches of the shunt VSI { and upper three switches of the series VSI in Fig. 1, the reduced nine-switch UPQC topology is achieved in . This configuration has a set of three shared switches as illustrated

Nine-switch UPQC topology.

The configuration features saving of three switches and performs satisfactorily under normal and sag conditions without an increase in the dc link voltage. However, it causes considerable rise in the switch current ratings of two switches per phase which is mainly attributed to the series connection of three switches in each leg (discussed in Section-IV). Therefore, six out of nine switches must be oversized for adequate operation of the nine-switch UPQC. In addition, all the nine switches must remain operational irrespective of the UPQC compensation mode. Thus, the reliability of the nine-switch UPQC reduces for a single switch malfunction.

PROPOSED TEN-SWITCH UPQC TOPOLOGY

In this paper, a new topology of UPQC, based on ten switches, is proposed for power quality enhancement applications. As depicted in Fig. 3, the proposed topology is realized by combining the phase C switches of shunt and series VSI { , } and { } in Fig. 1, respectively, into a common leg with a shared set of two switches and . Until now the ten-switch structure has been utilized in drives applications with certain limitations. The following subsection provides an overview of the ten-switch related work in the literature Proposed ten-switch UPQC topology.

Existing constraints and background work related to ten-switch structure

Like most reduced semiconductor topologies, ten-switch structure faces restriction on its allowable switching states for the shared leg (phase *C* in It can be clearly seen from that the output terminals for the shared leg “*C*” can be connected to either *V* or ground. Unlike the back-to-back configuration, the switching state where the upper terminal is connected to *V* and lower terminal is connected to ground (i.e. *VV* and) or vice-versa is not realizable as it will result in a direct short circuit of the dc bus. The blocking of two (out of four) states limits the dc link voltage available for the shared leg (“phase *C*”) to half of its value for back-to-back configuration.

Ten-switch configuration was earlier reported in to replace twelve-switch back-to-back converter for dual induction machine drive system. Although the configuration allows independent control of both machines with a wide range of variation in load torque and rotational speeds, it imposes a limitation on the dc link voltage. If and are the maximum values of phase-to- phase voltages at the terminals of the induction machine and , respectively, it is shown

Where *V* is the voltage across the dc link capacitor. In the special case of the following constraints can be established. Equation (2) implies that the dc link voltage must be doubled to achieve the maximum rotational speed for both machines simultaneously. Doubling of dc link voltage increases all the component stress by two folds, thus, offsetting the saving of two switches. For the same dc link voltage, the ten-switch structure leads to reduction in the terminal voltage and consequent speed range of both machines.

Attempts to enhance the dc-bus utilization for the ten-switch architecture have been reported in. The improvement reported, in , is obtained at the expense of identical operating (speeding and loading) conditions for both machines. In , the controller divides the dc link voltage by allocating predefined switching vectors to each machine. The restriction that the controller must have prior knowledge of the voltage profile for each machine makes the scheme impractical for variable industrial loads. In the ten-switch configuration is employed to drive the two induction motors in the center driven winders. It overcomes the limitation of dc link oversizing given by (1)-(2) due to 'inverse loading profile" of the two machines. When one motor operates at maximum speed, the other motor operates at minimum speed and vice versa. Since both motors increase/decrease speed in an alternate fashion, their voltage requirement is completely different (opposite). This allows the ten-switch system to remain operational for center driven winders utilizing the same dc link voltage required for back-to-back converter. However, the center driven winder is a special case and in general ten-switch configuration have not shown much economic value for dual motor drive systems.

Proposal

This paper proposes the use of ten-switch configuration as the most suitable candidate for shunt-series configuration, such as, UPQC. The rationale behind this recommendation is given below.

As shown in Fig. 3, the outputs of the upper VSI are connected to the PCC constituting the shunt configuration, whereas, the outputs of lower VSI are connected in series with the same PCC constituting the series configuration. The shared set of switches and are driven by the modulation signal which is calculated as follows.

Where and are the amplitude of the modulating signal for shunt and series VSIs, respectively. is the resultant modulating signal for the shared set of switches. Fig. 4(a) shows these details within the bandwidth of the dc link voltage in per unit (p.u) where corresponds to . To maintain the linear range of modulation for and the maximum allowable limit for is -1 to +1. This limit can be further stretched by 15% using third harmonic injection extending the linear range from to as shown in Fig. 4(b) and 4(d). Thus, up to 15% THD in the PCC voltage can be compensated without increasing the dc-link voltage. For higher values of voltage THD, (i.e.> 15%), like all existing configurations, the proposed topology will also require a higher dc-link voltage.

During normal condition, the shunt VSI supplies harmonic and fundamental reactive component of the load current while the series VSI injects the inverse of PCC voltage harmonics usually < 5% Since the shunt VSI operates at the same voltage level as PCC (1 p.u.), its reference signal amplitude is also unity. From (3), the amplitude of the reference signal for shared leg can go as high as 1.05 as shown in Fig. 4(a). If an ideal grid is considered (with no distortion in PCC voltage) the series VSI will simply operate with a modulation index of zero and .

Now consider that there is sag of magnitude V in the PCC voltage. On the occurrence of sag, the PCC voltage undergoes a reduction of . The shunt VSI modulation -101 (a) (b) m
index also decreases proportionally to the new value of (V). The series VSI compensates the sag by injecting a fundamental voltage given by VVV

Where V is the nominal load voltage. The new modulation index of the series VSI increases from 0.05 to . Fig. 4(c) reflects the transition in all three modulation indexes { from normal to sag mode of operation.

It can be observed from that the resultant modulation signal for the shared leg (phase *"C"*) does not extend out of the dc-link bandwidth during both (normal and sag) modes of operation. This is attributed to the fact that amplification in by any amount is always accompanied by a reduction in by the same factor. The self-tuning feature of both the modulation references causes the shared leg switches to always operate in the linear range of modulation. Thus, the proposal of the utilization of a ten-switch topology for UPQC can be concluded as the most suitable application. Figs. 4(b) and 4(d) reflect the operational area of the ten-switch UPQC for normal and sag mode of operations, respectively. The operating points in Fig. 4(b) and in Fig. 4(d) correspond to the normal mode in Fig. 4(a) and sag mode in Fig. 4(c), respectively.

Fig. 4 Modulation references transition for shared leg during normal (upper) and sag (lower) mode of operation in proposed configuration.

SWITCH RATING ANALYSIS

In section III, a subjective explanation is presented to use ten-switch configuration as UPQC. Despite its two switch saving feature, the effectiveness of the proposed ten-switch UPQC can only be evaluated after comprehensive analysis of its switch rating. Therefore, an analytical study is presented in this section to determine and compare the switch rating of the ten-switch UPQC with the twelve and nine-switch topologies.

From

Where h=1, 2, 3 is the harmonic order, i and i are the terminal currents of series and shunt VSIs, respectively. Considering the load current magnitude as the base and angle of the fundamental PCC voltage as the reference angle, transformer turns ratio n as unity, the series VSI current i is 1p.u as shown in the first part of (5). The shunt VSI current i consists of fundamental reactive and harmonic portion of load current. In the second part of (5), denotes the fundamental active component of load current whereas I accounts for the additional fundamental active component required to maintain the dc-link voltage. During steady state, I represents the loss component of the UPQC system and during sag condition, it also contains the active power component to achieve the overall power balance. For simplicity, neglecting the inverter losses and defining the sag depth as V The current I can be expressed as, $Iicsi$

From (6) it is clear that I is a function of the load power factor and sag depth during off nominal conditions. Furthermore, it can be observed from (5) that i and i have different magnitudes and phase angles.

Switch rating of back-to-back UPQC

Using the derivations given in, the switch current for the back-to-back UPQC of. is the half switching period of the carrier waveform. is the time interval during which the amplitude of carrier is higher than the modulating signal A amplitude. is the time interval during which the amplitude of modulating signal A is higher than the carrier. and are symbolic variables governing the unidirectional current through A and A . Based on (7), the maximum current rating of each switch in series VSI is (p.u) and shunt VSI is I (p.u). The voltage rating of each switch in the twelve-switch converter is same as the dc link voltage. Considering the nominal *rms*load voltage (as base, the dc link voltage would be (p.u).

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