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FIVE LEVEL FCMLI BASED STATCOM FOR SINGLE MACHINE INFINITE BUS SYSTEM

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ABSTRACT

The flying capacitor multilevel inverter (FCMLI) is a multiple voltage level inverter topology intended for high-power and high-voltage operations at low distortion. It uses capacitors, called flying capacitors, to clamp the voltage across the power semiconductor devices. A method for controlling the FCMLI is proposed which ensures that the flying capacitor voltages remain nearly constant using the preferential charging and discharging of these capacitors. A static synchronous compensator (STATCOM) and a static synchronous series compensator (SSSC) based on five-level flying capacitor inverters are proposed. Control schemes for both the FACTS controllers are developed and verified in terms of voltage control, power control, and power oscillation damping when installed in a single-machine infinite bus (SMIB) system. Simulation studies are performed using PSCAD/EMTDC to validate the efficacy of the control scheme and the FCMLI-based flexible alternating current transmission system (FACTS) controllers.

Index Terms: FCMLI, multilevel inverter, power oscillation damping, SMIB, SSSC, STATCOM.

INTRODUCTION

The multi level inverter was first introduced in 1975. The three level converters was the first multi level inverter introduced. A multilevel converter is a power electronic system that synthesizes a desired output voltage from several levels of dc voltages as inputs. With an increasing number of dc voltage sources, the converter output voltage waveform approaches a nearly sinusoidal waveform while using a fundamental frequency-switching scheme. The primary advantage of multi level inverter is their small output voltage, results in higher output quality, lower harmonic component, better electromagnetic computability, and lower switching losses.

The multilevel inverters have gained considerable interests over the past decade in industries as well as in academia over the multistep inverters and the conventional two-level inverters for high voltage and power applications. In the multilevel inverters, all the devices are individually controlled and hence can provide better control over voltage magnitude and harmonic suppression. Further, switching each device from a voltage that is a fraction of the total dc-link voltage avoids the problem of designing the costly and bulky snubber circuits.

The term multilevel starts with the three-level inverter. With the increase in levels the synthesized output waveform approaches the sinusoidal wave with minimum harmonic distortion. More levels also mean higher voltages can be spanned by series devices without device voltage sharing problems. Unfortunately, the number of achievable voltage levels is limited due to voltage unbalance problems, voltage clamping requirements, circuit layout, cost and packaging constraints .At present, there are three benchmark multilevel inverter topologies:

i) diode-clamped multilevel inverter (DCMLI), ii) cascade H-bridge inverter, and iii) flying capacitor multilevel inverter (FCMLI). DCMLI suffers from the limitations of dc-link voltage unbalance, indirect clamping of the inner

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devices and multiple blocking voltages of the clamping diodes. H-bridge cascade inverter has limitations such as the requirement of large number of inverters to decrease the harmonics and complex dc-voltage regulation loop. It needs separate dc sources for real power conversion and thus has somewhat limited applications.

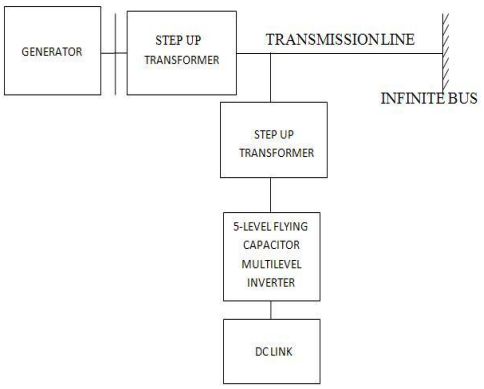
Connecting separate dc sources between two converters in a back-to-back arrangement (e.g., in UPFC) is not possible because a short circuit will be introduced when two back-to-back converters are not switching synchronously. In this inverter, the switching modulation needs to be optimized for high-performance applications due to a limited combination of switching patterns. Moreover, for reactive power exchange, the power pulsation at twice the output frequency occurring with the dc-link of each H-bridge inverter necessitates over-sizing of the link capacitors.

The FCMLI attempts to address some of the limitations imposed by the above-mentioned inverters. With the increase in the number of output voltage levels, the number of dc-link capacitors in cascade and in DCMLI increase and hence their control become more complex especially in transient conditions. However, the dc-capacitor control loop in FCMLI is as simple as in the conventional two-level inverter and is independent of the number of output voltage levels. The typical structure of FCMLI makes it possible to split the voltage constraints and to distribute them on several switches of smaller ratings in series. This also makes it possible to obtain a significant improvement of the output waveform and to increase the apparent frequency of this wave, allowing a significant reduction of the filtering requirements.

FIVE-LEVEL FCMLI BASED STATCOM

BLOCK DIAGRAM

This section describes the use of the STATCOM based on the five level flying capacitor inverter for power oscillation damping and voltage control of power system. The study is based on an SMIB system with the STATCOM connected in Shunt at the midpoint of the transmission line.



Block diagram of five-level FCMLI based STATCOM

BLOCK DIAGRAM DESCRIPTION

A STATCOM is a device that can provide reactive power support to a bus. It is useful in improving the transient stability, power oscillation damping, voltage stability, and increase in power transfer limit of the connected power system. It consists of a voltage source inverter connected to an energy storage device on one side and to the power system on the other side. A STATCOM can be viewed as a controllable ac voltage source, which appears behind a transformer leakage reactance.

The active and reactive power transfer is caused by the voltage difference across this reactance. Usually, the inverter output voltage is almost in phase with the voltage of the ac system. Therefore, only reactive power transfer occurs, whose quantity and sign depend on the magnitude of the inverter output voltage vis-à-vis that of midpoint ac voltage. If it is higher than ac voltage there active power is supplied to the system and if it is lower the converter circuit absorbs the reactive power. The magnitude of the inverter output voltage depends on the modulation index and the dc-link voltage.

BLOCK DIAGRAM OF STATCOM CONTROL

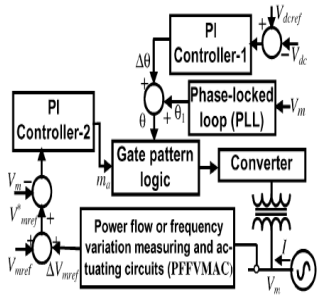
There are many strategies to control the operation of STATCOM such as PI control, pole placement control and linear quadratic control The PI control scheme has been used here to study the performance of the system. In normal operation, for the voltage control of a bus, the value of Vm_{ref} depends on the desired voltage profile at that particular bus; therefore, the power flow or frequency variation measuring and actuating circuits (PFFVMAC) are not needed. The PFFVMAC block is needed when some feedback signal is taken from the power system for improving the transient stability of the system.

There are two Control objectives in the STATCOM control: ac-bus voltage control and dc-link voltage control. Therefore, two internal control loops containing two PI controllers are used here. The dc capacitor voltage is regulated around a reference value $Vdc_{ref,}$ which is kept fixed and is chosen considering the rating of the STATCOM.

Since the output voltage of the inverter and V_m should be in phase, a phase locked loop (PLL) is used that has V_m as input and angle Q_1 as output. Ideally, for pure reactive power exchange between the compensator and the line, the dc link voltage should remain constant. However, the capacitor discharges due to losses in switching, snubbed circuits, and in transformers. Therefore, to keep the capacitor voltage constant, some amount of real power exchange is needed between the inverter and the ac system.

The PI controller-1, with an input of the error between V_{dc} ref and V_{dc} and output Δ_{Q} facilitates this power exchange. If the inverter output voltage is made to lag the voltage of the ac system then the active power flow is from the ac system to the dc side of the inverter charging the capacitor. The reverse will happen when the corresponding phase relation is reversed. Another control loop (PI contoller-2) generates the modulation index. The input to this PI controller is the difference between the reference rms value V_{mref} and the actual rms value of the voltage V_m at the point of connection.

BASIC CONFIGURATION OF A FIVE-LEVEL FLYING CAPACITOR INVERTER



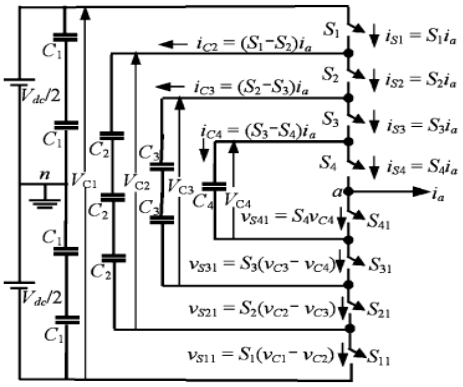


Fig 4.3 shows one phase of a five-level flying capacitor inverter. In the figure each switch $s_1$tos$_4$ and s_{11}tos$_{41}$ consists of a power semiconductor switch and an anti parallel diode. The pairs of the switches ($s_{1,}$ s_{41}), ($s_{2,}$ s_{21}), ($s_{3,}$ s_{31}), and ($s_{4,}$ s_{41}) are closed in complementary manner. Thus, if s_1 is ON, s_{11} is OFF and vice-versa.

Each capacitor shown in the figure is of equal voltage rating. Let us consider the group of capacitors in a single clamping leg as one equivalent capacitor and call them $C_{1,}$ C_2, C_3, and C_4. ThenC_1, is the main dc link capacitor, this is required to be regulated externally. Therefore, either a battery of suitable rating is connected in place of C_1 (or) C_1 without the battery connected across it is regulated around a reference dc-link voltage using the real power exchange from the line. For a three-phase inverter two more phases of the same construction are coupled to the same dc-link.C_2, C_3, and C_4 are flying capacitors that provide the multilevel voltage ability to the converter. The flying capacitors of one phase are independent from those of other phases. If the voltage V_{C1} is V_{dc}, then V_{c2}, V_{c3}, and V_{c4} are $3V_{dc}$/

4, V_{dc} /2 , and V_{dc} /4 , respectively. For any initial state of clamping voltages the inverter output voltage is given by

$$V_{an} = S_1(V_{C1} - V_{C2}) + S_2(V_{C2} - V_{C3}) + S_3(V_{C3} - V_{C4}) + S_4V_{C4} - V_{C1}/2.$$

SWITCHING SCHEME FOR A FIVE-LEVEL FCMLI

S_1	S_2	S_3	S_4	C_2	C_3	C_4	V_{an}
ON	ON	ON	ON	NC	NC	NC	$+V_{dc}/2$
ON	ON	ON	OFF	NC	NC	+	$+V_{dc}/4$
ON	ON	OFF	ON	NC	+	-	
ON	OFF	ON	ON	+	-	NC	
OFF	ON	ON	ON	-	NC	NC	
OFF	OFF	ON	ON	NC	-	NC	0
OFF	ON	OFF	ON	-	+	-	
OFF	ON	ON	OFF	-	NC	+	
ON	OFF	OFF	ON	+	NC	-	
ON	OFF	ON	OFF	+	-	+	
ON	ON	OFF	OFF	NC	+	NC	
ON	OFF	OFF	OFF	+	NC	NC	$-V_{dc}/4$
OFF	ON	OFF	OFF	-	+	NC	
OFF	OFF	ON	OFF	NC	-	+	
OFF	OFF	OFF	ON	NC	NC	-	
OFF	OFF	OFF	OFF	NC	NC	NC	$-V_{dc}/2$

Table Switching Scheme

In Fig 4.3 and in (1), the switching states S_1toS_4 take the value 1 if the corresponding switch is conducting and 0 otherwise. Based on (1), the switch combinations given in Table I are used to synthesize the output voltage V_{an} of phase-a with respect to the neutral point n. Table I also indicates the states of the flying capacitors corresponding to the switching combinations chosen. The neither state NC indicates that the capacitor neither charges nor discharges in this mode. The states +and - denote the charging and discharging respectively of the corresponding capacitors. The switching states given are for the positive half cycle of the current waveform (indicated as outgoing current in Fig 4.3).

The capacitor states (+and -) will reverse for the negative half cycle of the current. In general, an n-level FCMLI requires (n-1) pairs of power semiconductor devices and (n-1)*(n-2)/2clamping capacitors per phase leg in addition to(n-1) main dc bus capacitors provided all the capacitors are of equal value. The number of capacitors can be reduced by sizing the capacitors in a single leg as an equivalent one. The size of the voltage increment between two consecutive clamping legs defines the size of voltage steps in the output waveform.

The voltage of the innermost clamping leg (e.g.C_4 in Fig 4.3) clamping the innermost two devices is V_{dc} /(n-1) . The voltage of the next innermost clamping leg will be V_{dc} /(n-1) + V_{dc} /(n-1) =2V_{dc} /(n-1) and so on. Thus, each next clamping leg will have the voltage increment of V_{dc} /(n-1) from its immediate inner one. The voltage

stress across each capacitor is V_{dc} /(n-1).The voltage levels and the arrangements of the flying capacitors in the FCMLI structure assure that the voltage stress across each main device is same and is equal to V_{dc}/(n-1) .

The line-to-line output voltage of the inverter varies from +V_{dc} to- V_{dc} and has (2n-1) levels in the output, while the phase voltage varies from +V_{dc} to- V_{dc} with n-levels. It can be seen from Table I that the structure offers multiple switching combinations for $V_{an=}$ V_{dc} /4,0 and- V_{dc} /4. Since such redundancies are available, one can choose a preferential switching state that will help in maintaining the capacitor voltages constant. However, the switching combination chosen affects the current rating of the capacitors. In the other two combinations more than one capacitor are required to be charged or discharged.

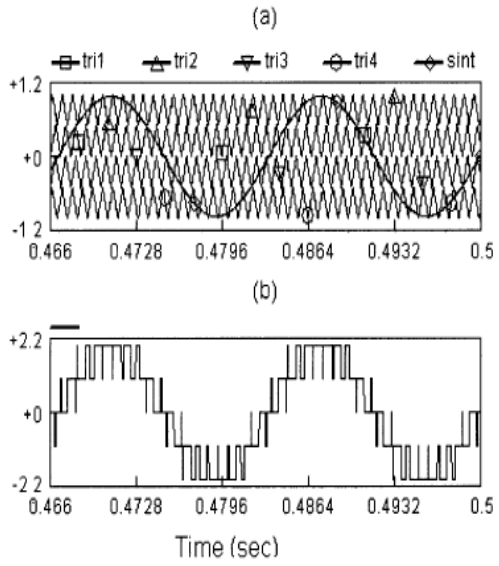
MODULATION SCHEME

There are the various strategies developed to improve the output voltage and reduce the harmonics, sinusoidal pulse width modulation (SPWM) strategy is employed here. In this method for an n-level inverter, (n-1) carrier waves are compared with a controlled sinusoidal modulating signal and the switching rules for the switches are decided by their intersections. The output signal of the comparator resembles with the output voltage waveform of the inverter and decides the voltage level that must be generated at a particular instant.

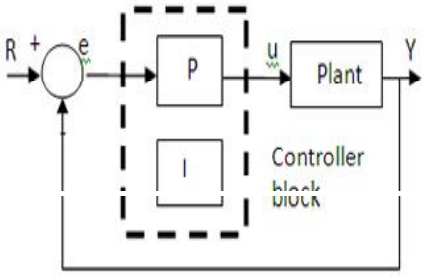
For a five level inverter, a modulating signal and 4 carrier waves are required for each phase of the inverter as shown in Fig 4.4. The modulating signals of each phase are displaced from each other by 120 degree. The phase shift angle of the modulating signal, i.e. ϴ, depends on the application requirements. The modulation index m_a is given by

$$m_a = A_m/2A_c$$

where $A_m$is the amplitude of the modulating signal and A_c is that of one carrier wave (peak to peak). Here, the carrier waves are taken to have phase displacement of 120 for smallest distortion in the output and their frequency is taken as n_c times to that of the modulating signal, where n_c is a multiple of three so that triplen harmonic cancellation takes place across the three-phase inverter load .



Modulation scheme. (a) SPWM. (b) Output waveform.

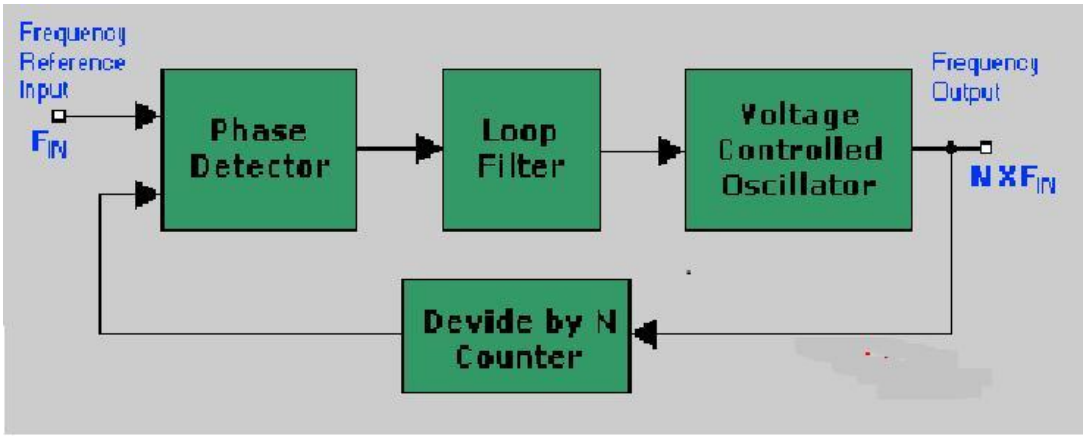


The carrier waves and the modulating signals are compared and the output of the comparator defines the output voltage waveform. It is assumed that the modulating signal varies from +0.98 to -0.98. The amplitudes of the four carrier waves are from 0 to 0.5, 0.5 to 1, in the positive half cycle of the modulating signal, and from 0 to to-0.5, -0.5 to -1, in the negative half cycle. The comparator output is +1when the modulating signal exceeds the carrier wave and zero otherwise.

PROPORTIONAL-INTEGRAL (PI) CONTROL

The combination of proportional and integral terms is important to increase the speed of the response and also to eliminate the steady state error.

Fig Block diagram of Proportional Integral (PI) controller



The proportional and integral terms is given by

$$u(t) = K_p e(t) + K_i \int e(t)dt$$

K_p and K_i are the tuning knobs, are adjusted to obtain the desired output. The following speed control example is used to demonstrate the effect of increase/decrease the gain, K_p and K_i. A DC motor dynamics equations are represented with second order transfer function,

$$G(s) = \frac{\dot{\theta}}{V} = \frac{K_t}{(Js+b)(Ls+R) - K_e K_t}$$

Where,

$K_t = K_e$ = electromotive force constant = 0.01Nm/Amp
b = damping ratio of the mechanical system = 0.1Nms
J = moment of inertia of the rotor = $0.02 kgm^2s^{-2}$
R = electric resistance = 1Ω
L = electric inductance = 0.5H

After we include the PI controller, the closed-loop transfers function become

$$G_p(s) = \frac{Y}{R} = \frac{K_t K_p}{(Js+b)(Ls+R) - K_e K_t - K_t K_p}$$

PHASE LOCKED LOOP

PLL stands for *'Phase-Locked Loop'* and is basically a closed loop frequency control system, which functioning is based on the phase sensitive detection of phase difference between the input and output signals of the controlled oscillator (CO). The Phase Locked Loop method of frequency synthesis is now the most commonly used method of producing high frequency oscillations in modern communications equipment. Phase locked loop systems to generate stable high frequency oscillations. Fig 4.6 shows the classic configuration phase locked loop. The phase detector is a device that compares two input frequencies, generating an output that is a measure of their phase difference (if, for example, they differ in frequency, it gives a periodic output at the difference frequency). If f_{IN} doesn't equal f_{VCO}, the phase-error signal, after being filtered and amplified, causes the VCO frequency to deviate in the direction of f_{IN}. If conditions are right, the VCO will quickly "lock" to f_{IN} maintaining a fixed relationship with the input signal.

At that point the filtered output of the phase detector is a dc signal, and the control input to the VCO is a measure of the input frequency, with obvious applications to tone decoding (used in digital transmission over telephone lines) and FM detection. The VCO output is a locally generated frequency equal to f_{IN}, thus providing a clean replica of f_{IN}, which may itself be noisy. Since the VCO output can be a triangle wave, sine wave, or whatever, this provides a nice method of generating a sine wave, say, locked to a train of pulses.

In one of the most common applications of PLLs, a modulo-*n* counter is hooked between the VCO output and the phase detector, thus generating a multiple of the input reference frequency f_{IN}. This

is an ideal method for generating clocking pulses at a multiple of the power-line frequency for integrating A/D converters (dual-slope, charge-balancing), in order to have infinite rejection of interference at the power-line frequency and its harmonics. It also provides the basic technique of frequency synthesizers.

CONCLUSION

In this project, a proposal has been made for shunt compensations based on five-level flying capacitor inverter. The basic concepts and operational features of the inverter have been explored. A control scheme has been proposed which uses the preferential charging or discharging of flying the capacitors to balance their voltages. The control scheme allows balanced flying capacitor voltages and, hence, output phase and line voltages as desired with much less THD using the SPWM.

The simulation results verify the control scheme proposed. A STATCOM has been simulated based on the five-level inverter. The proposed STATCOM generate output voltage waveform with lower harmonic distortion and allow higher power handling capability. The performances of the compensator have been investigated on an SMIB system, subjected to a bolted three-phase fault. The simulation results confirm that the proposed STATCOM have satisfactory performances.

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