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A UNIDIRECTIONAL MULTI-LEVEL SINGLE PHASE BRIDGELESS RECTIFIER TARGETING HIGH EFFICIENCY

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ABSTRACT

This paper with new multi-level unidirectional single-phase PFC rectifier topology is well-suited for applications targeting high efficiency and/or high power density. The characteristics of a selected novel rectifier topology, including its principles of operation, feedback control scheme, and a power circuit design related analysis are presented which include remarkably low switching losses and single ac side, boost inductor. To improve the characteristic and enable the use of higher switching frequencies, multilevel converters can be employed to build power factor correction rectifier topologies. With the multi-level topologies the losses are typically much lower since the voltage steps over the boost inductor are only one half of the dc-link voltage. Thus, the inductance and the size of the boost inductor are reduced. This achieve high power factor with reduced conduction and commutation losses which can be used for telecommunication applications. The reduction in conduction losses occurs because the proposed topology presents less power semiconductors in the current path. Thus the efficiency of the proposed topology tends to be higher since conduction losses will be lower.

Keywords*:* Single phase, PFC, Topology, Frequencies, Voltage.

INTRODUCTION

An unidirectional high power factor single-phase ac-dc system assembled by cascading a single-phase diode bridge and a boost dc-dc converter is employed. This converter system, known as conventional single-phase power factor correction (PFC) boost-type rectifier, is used for power conversion below 1 kW, this circuit needs to operate at high switching frequencies, which can lead to unacceptably high switching losses since the switch and diode must commutate the full dc-link voltage. This ac-dc converter typically features low production cost. Unfortunately, the current across inductor is carried through three semiconductor devices in every operation stage, high conduction losses.

Hence in this context, bridgeless PFC rectifiers are appropriate solutions regarding conduction losses. This is because in this model only two devices conduct current in at least one of their current conduction states. This characteristic can expressively enhance the conduction loss performance in many systems especially for power

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conversion levels above 1 kW. However, the power semiconductor devices in these converters must typically withstand and commutate the full dc-link voltage and, thus, present appreciable switching losses. To improve this characteristic and enable the use of higher switching frequencies, multilevel converters can be employed to build PFC rectifier topologies.

The new topologies present a lower number of semiconductors in the current paths when compared with the conventional circuits. Additionally, the proposed rectifier system avoids the use of selective switches and allows low conduction losses for wide operation range. Furthermore, even though some of the semiconductors are to be rated to withstand the full dc-link voltage, all commutations occur under half of the dc-link voltage.

This leads to reduced switching losses. Even though the number of semiconductors is substantially increased for the proposed ac-dc converters when compared to two-level solutions these topologies are indicated where very high efficiency and/or switching frequencies are required. The passive components losses are typically dominated by the boost inductor. With the multi-level topologies these losses are typically much lower since the voltage steps over the boost inductor are only one half of the dc-link voltage. Thus, the inductance and the size of the boost inductor are reduced.

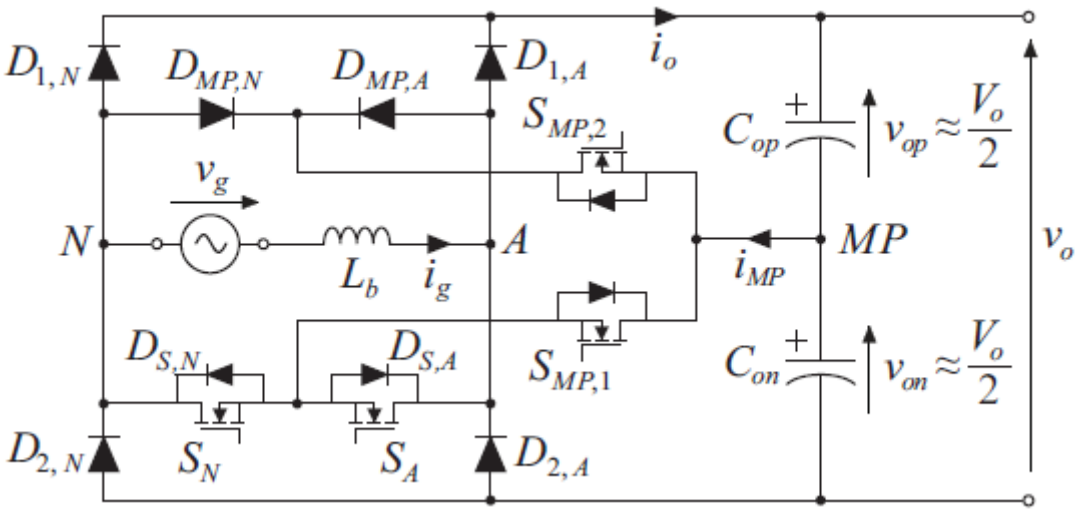
Hence the proposed multilevel PFC rectifier is a very attractive solution for applications in single phase Power supplies targeting for high efficiency, high line power quality and high power density.

The term multilevel began with the three-level converter. Here the five level concepts are used. The elementary concept of a multilevel converter is to achieve higher power with the use of a series of power semiconductor switches with several lower voltage dc sources to perform the power conversion by synthesizing a staircase voltage waveform.

The commutation of the power switches aggregate these multiple dc sources in order to achieve high voltage at the output; however, the rated voltage of the power semiconductor switches depends only upon the rating of the dc voltage sources to which they are connected. A multilevel converter has several advantages over a conventional two-level converter that uses high switching frequency PWM.

Multilevel converters not only can generate the output voltages with very low distortion, therefore the electromagnetic compatibility (EMC) problems can be reduced. Multilevel converters can operate at both fundamental switching frequency and high switching frequency PWM. It produces lower switching frequency which usually means lower switching losses and higher efficiency.

CIRCUIT DIAGRAM



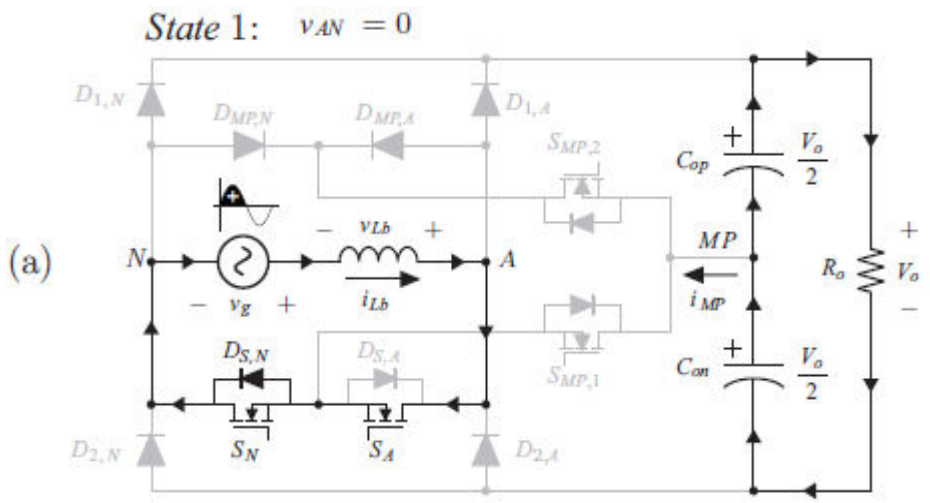
CIRCUIT DIAGRAM OF PROPOSED SYSTEM

The single-phase boost-type PFC rectifier depicted utilizes four active switches (S_A, S_N, $S_{MP;1}$ and $S_{MP;2}$), and six discrete diodes ($D_{MP;N}$, $D_{MP;A}$, $D_{1;N}$, $D_{1;A}$, $D_{2;N}$ and $D_{2;A}$). Diodes $D_{1;N}$, $D_{1;A}$, $D_{2;N}$ and $D_{2;A}$ are fast-switched devices, i.e., will be required to commutate under current, while the diodes $D_{MP;N}$ and $D_{MP;A}$ and the body diodes of S_N and S_A are switched off by $S_{MP;1}$ and $S_{MP;2}$.

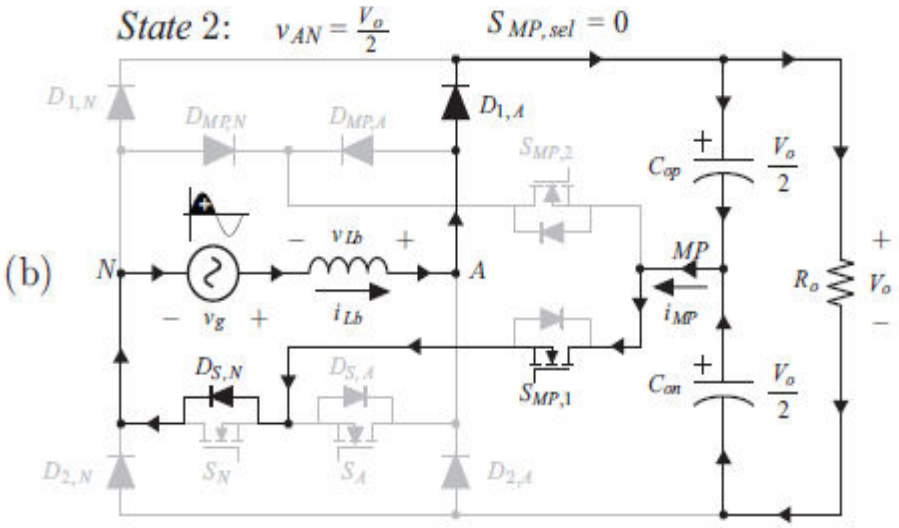
Therefore, $D_{MP;N}$ and $D_{MP;A}$ can be implemented with standard fast or ultrafast silicon diodes with relatively low forward voltage drop, while the four bridge diodes would benefit from Sic or GaN semiconductor technology. The intrinsic diodes of the MOSFETs S_A and S_N ($D_{S;\,A}$ and $D_{S;\,N}$) are used in the circuit operation and can profit from the low forward voltage drop body diode characteristics of super junction MOSFETs. Interestingly, the switches S_A, S_N and $S_{MP;\,1}$ have the same reference for their gate command, which simplifies and reduces the cost of isolated gate drive circuits.

RECTIFIER CURRENT CONDUCTION STATES FOR POSITIVE INPUT CURRENT (I_{Lb} >0)

The rectifier conducts current during both positive and negative input currents, i_{Lb}, respectively. The dc-link is constructed with two series connected capacitors that allow the formation of five voltage levels across the terminals A and N ($V_{A;N}$ = 0, ±Vo/2, or ±Vo).



For improved conduction losses while implementing the state $V_{A;N}= 0$, the switches $S_{MP;1}$ and $S_{MP;2}$ could also be turned on together with S_A and S_N. In this case, two parallel paths across the semiconductor are created for the impressed current. Alternatively, the state $V_{A;N} = 0$ could also be implemented by solely turning on $S_{MP;1}$ and $S_{MP;2}$, while all the remaining active devices are switched off.



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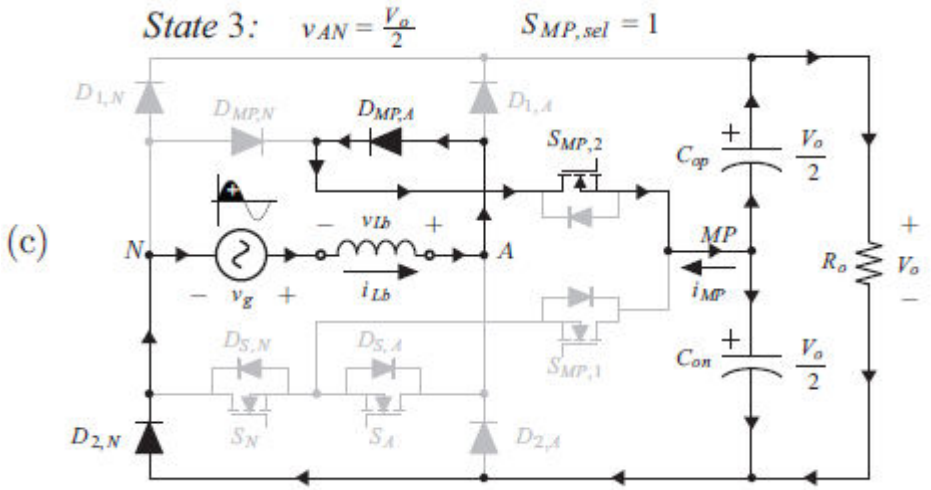
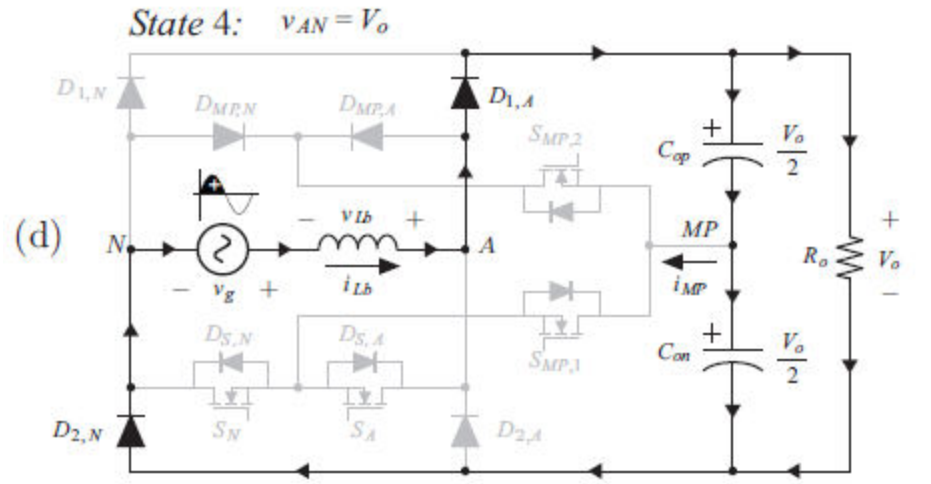
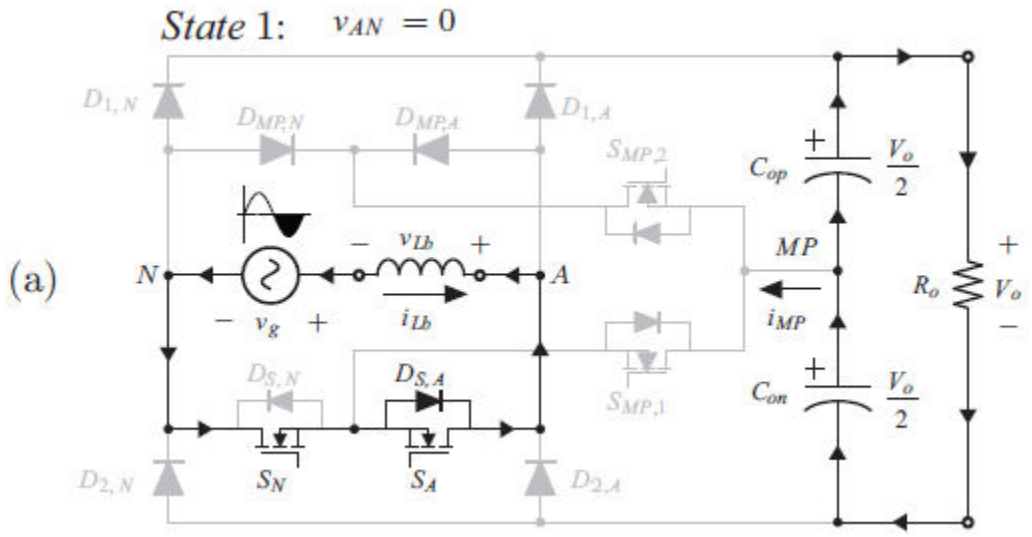


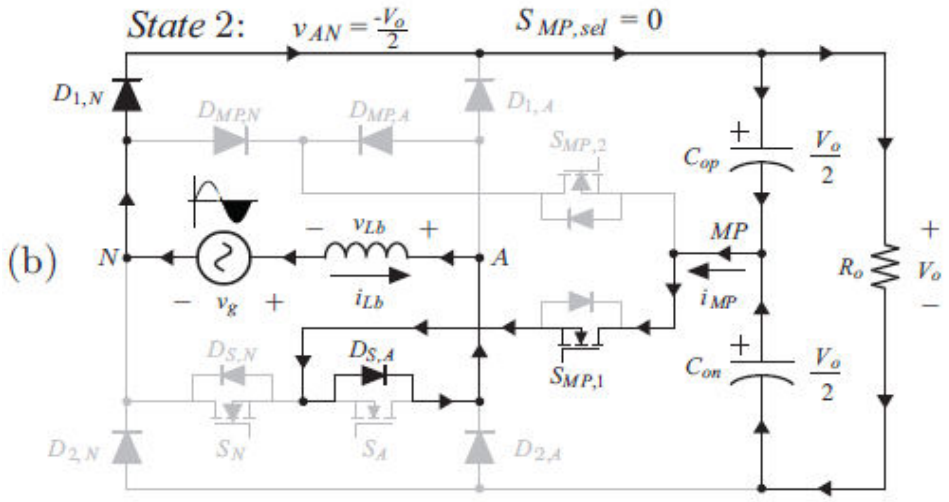
There are two redundant switching states for the formation of V_{AN} = ±Vo/2 (states 2 and 3), which results in different current i_{MP} direction across the midpoint MP of the output capacitors C_{op} and C_{on}. Hence, this feature can be used for balancing the voltages across the dc-link capacitors. Enabling $S_{MP;1}$ charges C_{op} and discharges C_{On}, while the opposite occurs if $S_{MP;2}$ conducts

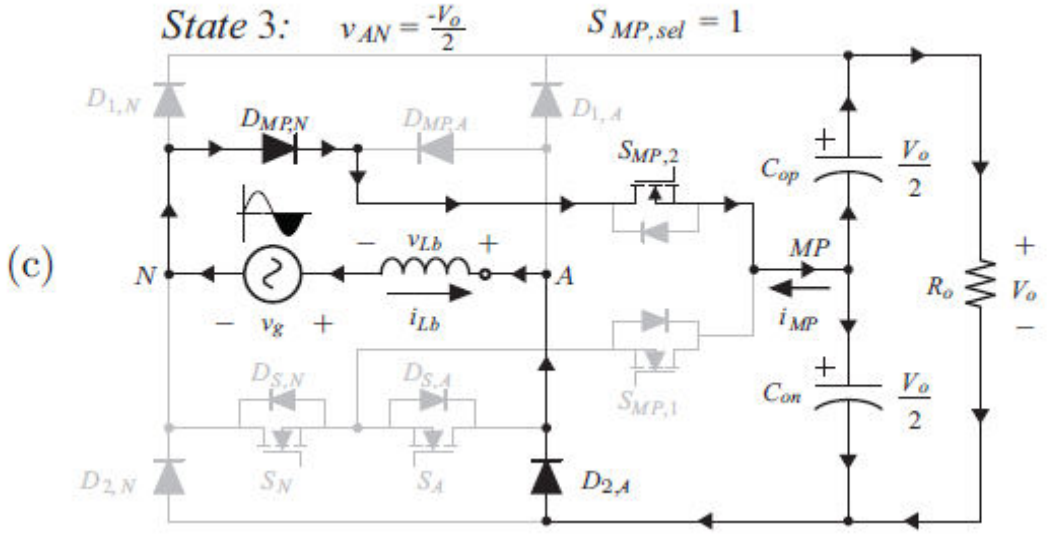


RECTIFIER CURRENT CONDUCTION STATES FOR NEGATIVE INPUT CURRENT (I_{Lb} <0)



For improved conduction losses while implementing the state $V_{A;N}$ = 0 , the switches $S_{MP;1}$ and $_{SMP;2}$ could also be turned on together with S_A and S_N. In this case, two parallel paths across the semiconductors are created for the impressed current. Alternatively, the state $V_{A;N}$ = 0 could also be implemented by solely turning on $S_{MP;1}$ and $S_{MP;2}$, while all the remaining active devices are switched off.





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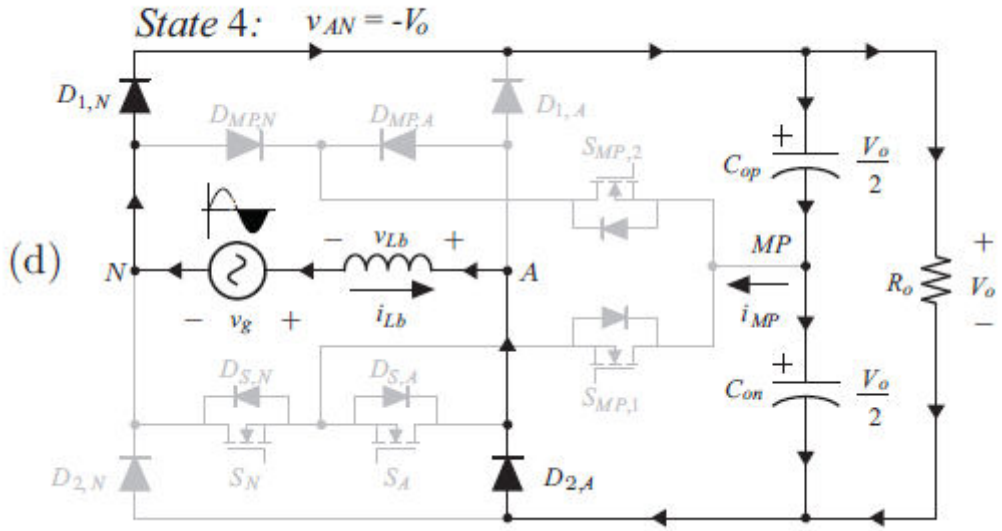
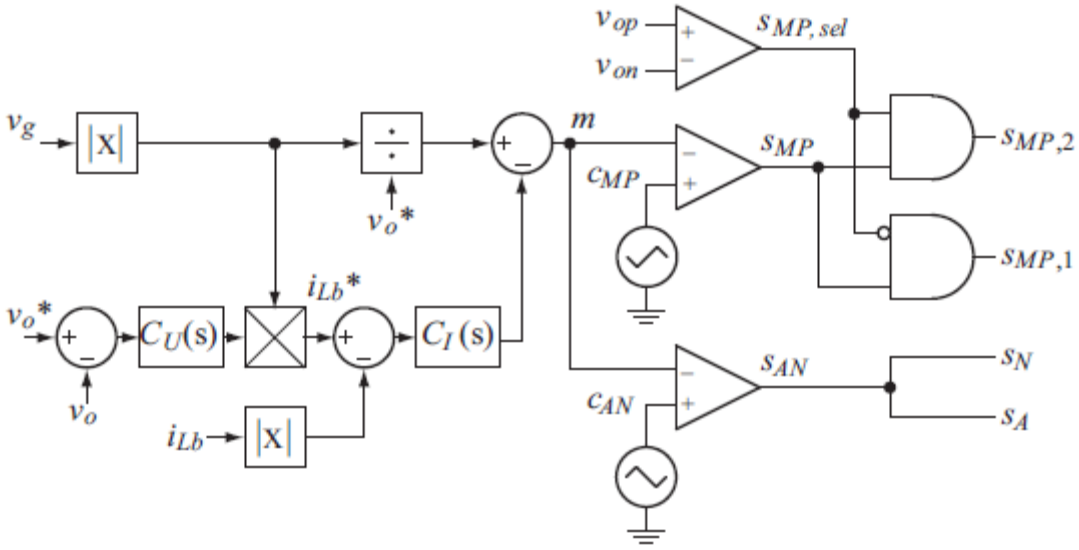


The external characteristics of these topologies are equivalent. However, the efficiency of the proposed topology tends to be higher since conduction losses will be lower. This reduction in

conduction losses occurs because the proposed topology presents less power semiconductors in the current path, except in the ±Vo states during both positive and negative conduction states.

PWM MODULATION AND FEEDBACK CONTROL SCHEME

A suitable feedback control scheme able to regulate the output voltage of converter, v_O, and shape the ac-side current i_{Lb}. Therein, a slow outer control loop is used to regulate the output voltage v_o to a constant reference voltage v_o* and to generate a reference signal i_{Lb}* for the fast inner current control loop with similar waveform shape of the rectified input voltage v_g. Additionally, a logic signal $S_{MP;\,sel}$ is used to guide the selection of the redundant current conduction state (state 2 and 3) in order to balance the partial dc-link voltages, v_{op} and v_{on}.



FEEDBACK CONTROL AND PWM MODULATOR CIRCUIT

The gate commands for S_A, S_N, $S_{MP};1$ and $S_{MP};2$ are guided by the logic signals S_{AN} and S_{MP} which are generated by comparing the feedback control signal m with the two interleaved triangular carriers C_{AN} and C_{MP}. In the proposed PWM modulator, the transition of the signal $S_{MP;sel}$ is synchronized with the peak of C_{AN} in order to reduce the switching losses across $S_{MP};1$ and $S_{MP};2$ for m < 1=2. In this case, due to the 180˚ phase-shift between C_{AN} and C_{MP} the transition between states 2 and 3 occurs after passing through an intermediate state (state 1), ensuring the commutation of $S_{MP};1$ and $S_{MP};2$ under zero current.

Although it is possible to set the converter operation $V_{A;N}$ = 0 by solely switching S_A when i_{Lb} is positive or by only gating S_N for negative i_{Lb}, these switches are always simultaneously commanded in the suggested scheme, following the comparison between m and

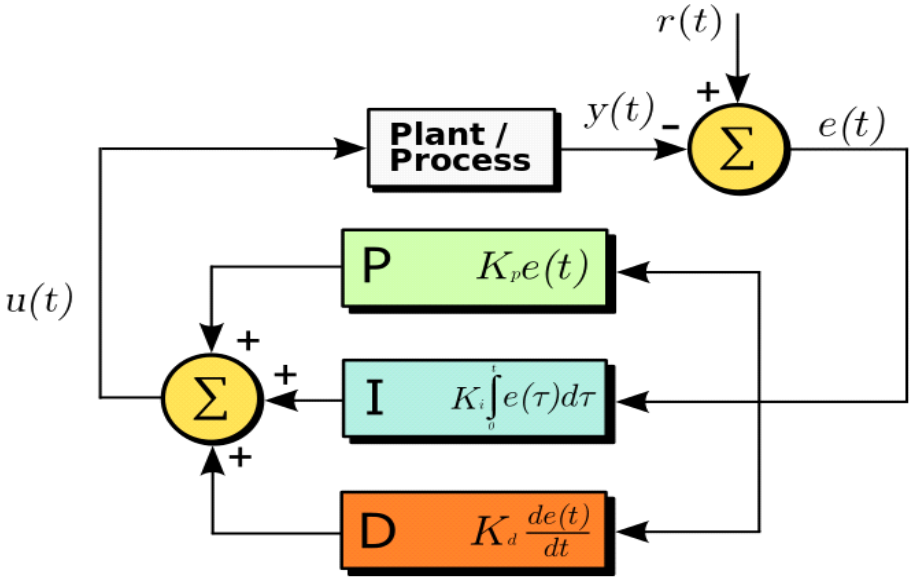
C_{AN}. This logic reduces the conduction losses across the MOSFETs S_A and S_N and also simplifies their command circuits. Here PID controller is used.

PID CONTROLLER

The PID controller algorithm involves three separate constant parameters, and is accordingly sometimes called three-term control: the proportional, the integral, the derivative values, denoted as P, I and D. Simply put, these values can be interpreted in terms of time: P depends on the present error, I on the accumulation of past errors, and D is a prediction of Future errors, based on current rate of change.

The weighted sum of these three actions is used to adjust the process via a control element such as the position of a control valve, a damper the power supplied to a heating element.

By tuning the three parameters in the PID controller algorithm, the controller can provide control action designed for specific process requirements. The response of the controller can be described in terms of the responsiveness of the controller to an error, the degree to which the controller overshoots the set point, and the degree of system oscillation. Note that the use of the PID algorithm for control does not guarantee optimal control of the system or system stability.



PID CONTROLLER

PFC RECTIFIER DESIGN ANALYSIS FREQUENCY SPECTRA

The five-level ac-side voltage v_{AN}, also known as the rectifier differential mode voltage (DM), for the proposed modulation strategy is defined where the amplitudes of the frequency harmonics can be found.

The proposed PFC rectifier presents reduced spectra amplitudes and, thus, leads to smaller EMC filter components for, both, CM and DM when compared to the bridgeless rectifier. Its conducted emissions generation performance in this regard is comparable to that of an interleaved bridgeless PFC converter with the advantage of using a single inductor. On the other hand, the proposed topology might present higher CM voltage than the conventional boost rectifier since it, as in the case of the bridgeless, does not feature the negative point of the line being always connected to the negative dc bus through some rectification diode. The final CM noise paths will strongly depend on the parasitic elements of the circuit and the analysis of CM spectra presents only part of the required analysis. The proposed topology will typically present a larger CM filter and a smaller DM filter than the conventional PFC rectifier.

EFFICIENCY COMPARISON

The MOSFET parameters in this case are adjusted to half the resistance values and double the capacitance values. All curves do not consider passive components losses and signal electronics consumption.

_ 300-V MOSFETs ($S_{MP;1}$, $S_{MP;2}$): Si MOSFET STW75NF30.

_ Diodes in series with MOSFETs ($D_{MP;A}$, $D_{MP;N}$): Si diodes RURP3060.

The comparison does not include the passive components losses and it is assumed that no reverse recovery occurs. The rms value of the input voltage is 220 V, frequency is 60 Hz, output voltage is 380 V and the output power is 3 kW. The switching losses are computed based on the switching times calculations.

However, as the switching frequency rises, the efficiency of the three-level bridgeless is not as affected and from approximately 80 kHz on the proposed topology produces lower total losses. This would be more pronounced if the boost inductor and EMC filter elements were considered. The voltages across the MOSFETs are presented; where it is noted that all commutations occur with a voltage level equivalent to half the output voltage, even at the switches that need to block the full dc-link voltage. This produces low switching losses.

TOTAL HARMONIC DISTORTION

The total harmonic distortion, or THD, of a signal is a measurement of the harmonic distortion present and is defined as the ratio of the sum of the powers of all harmonic components to the power of the fundamental frequency.THD is used to characterize the linearity of audio systems and the power quality of electric power systems.

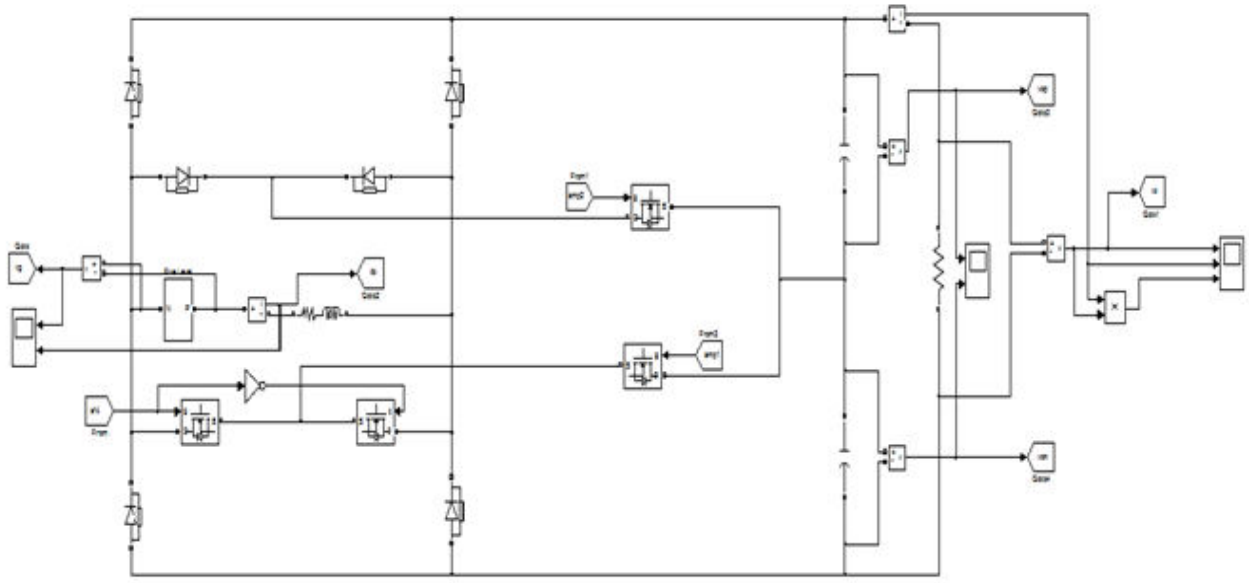
Total harmonic distortion, or THD, is the summation of all harmonic components of the voltage or current waveform compared against the fundamental component of the voltage or current wave:

$$THD = \frac{\sqrt{(V_2^2 + V_3^2 + V_4^2 + \cdots + V_n^2)}}{V_1} * 100\%$$

The formula above shows the calculation for THD on a voltage signal. The end result is a percentage comparing the harmonic components to the fundamental component of a signal.

Harmonics have frequencies that are integer multiples of the waveform's fundamental frequency. For example, given a 60Hz fundamental waveform, the 2nd, 3rd, 4th and 5th harmonic components will be at 120Hz, 180Hz, 240Hz and 300Hz respectively.Here at full power a high power factor (φ = 0.99) and a low input current THD (THD=2.18%) have been measured.

SIMULATION MODEL



SIMULATION MODEL OF MULTI-LEVEL BOOST TYPE PFC RECTIFIER

In this proposed model a single phase five level input is fed to the boost type power factor correction rectifier topology. The rectifier conducts current for both positive and negative

input current. The input voltage and current is fed to the active and reactive power block in order to help of power factor correction block where the mathematical operation is carried out and finally power factor of nearly unity is obtained. The dc-link is constructed with two series connected capacitors that allow the formation of five voltage levels across the terminals A and N ($V_{A;N}$ = 0, ±Vo/2, or ±Vo). There are two redundant switching states for the formation of $V_{A;N}$ = ±Vo/2 which results in different current direction across the midpoint MP of the output capacitors C_{op} and C_{on}.

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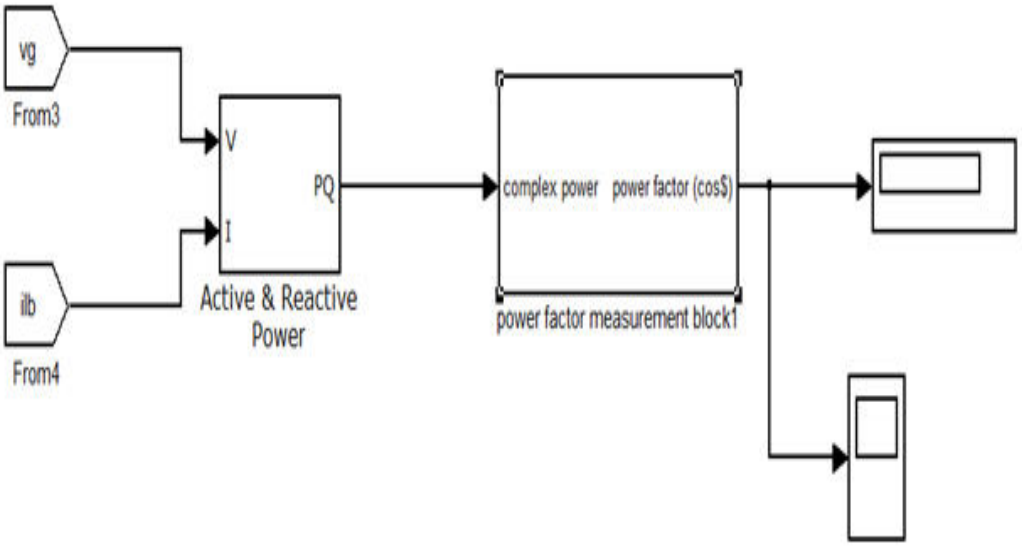
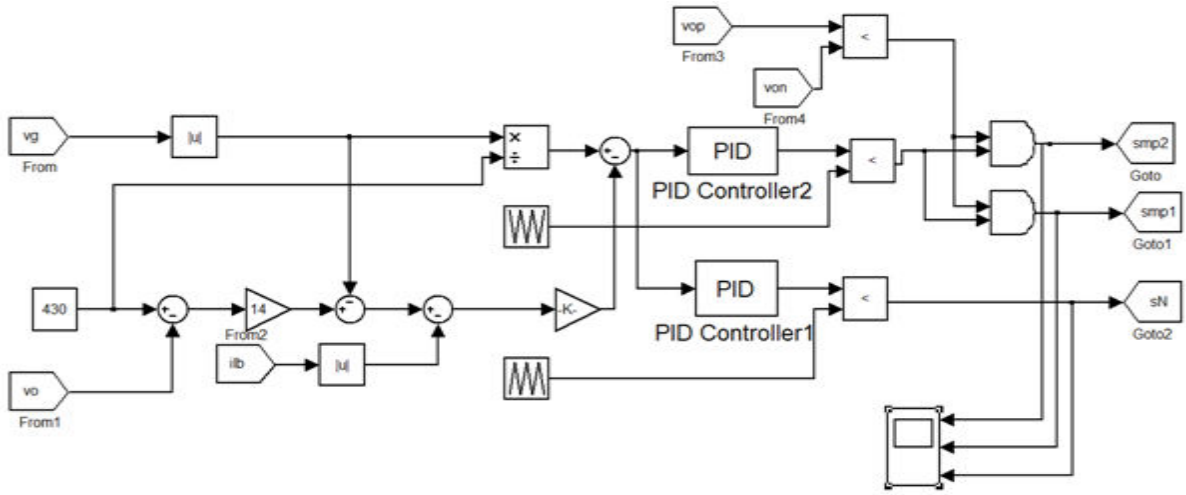
POWER FACTOR CORRECTION MODEL



SIMULATION MODEL OF POWER FACTOR CORRECTION

A suitable feedback control scheme is implemented using a PID controller in order to regulate the output voltage of the converter and shape the ac side current. The outer control loop is used to regulate the output voltage v_o to a constant reference voltage v_o* and to generate a reference signal i_{Lb}* for the inner current control loop with similar waveform shape of the rectified input voltage v_g. With the help of pulse width modulation technique the gate commands for S_A, S_N, $S_{MP;1}$ and $S_{MP;2}$ are found, which is guided by the logic signals S_{AN} and S_{MP} which are generated by comparing the feedback control signal with the two interleaved triangular carriers C_{AN} and $C_{MP.}$ This logic signal reduces the conduction losses across the MOSFETs.

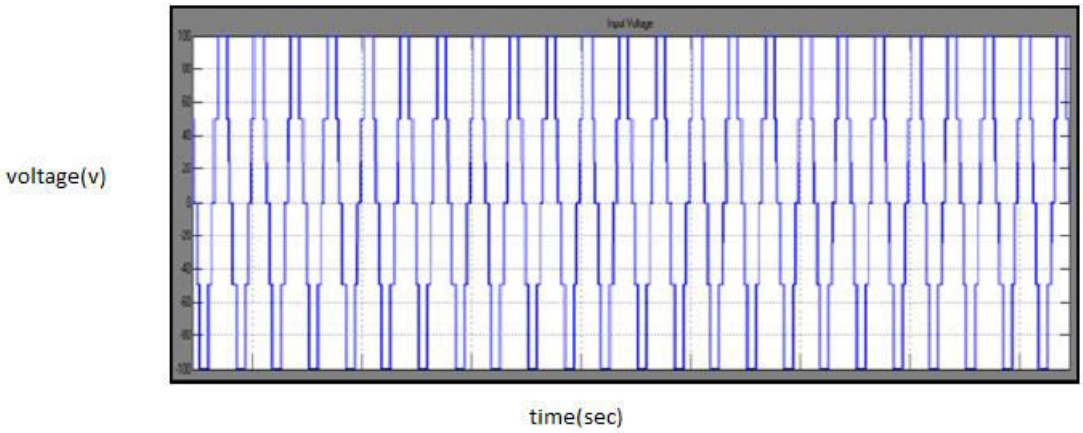
PID CONTROLLER MODEL



SIMULATION MODEL OF PID CONTROLLER

RESULTS

SIMULATION INPUT WAVEFORM



WAVEFORM OF INPUT VOLTAGE

Here five-level voltage of 100V is fed as input voltage and 3A current is fed as input current to the power factor correction boost type rectifier where it produces nearly unity power factor and the boost type rectifier tends to boost up the voltage(i.e., output voltage tends to be higher than the input voltage).

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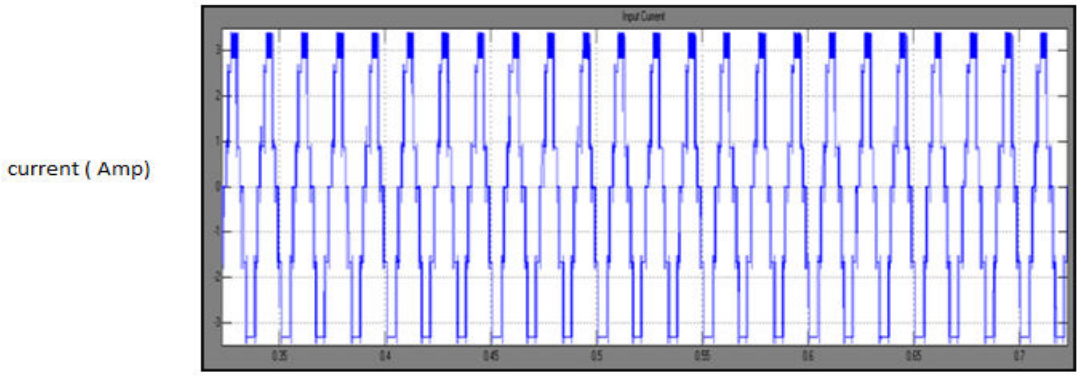
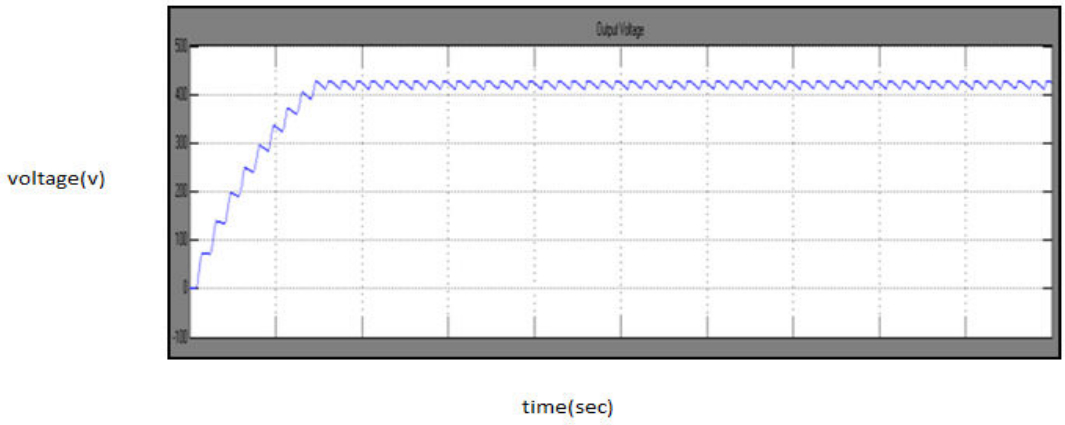
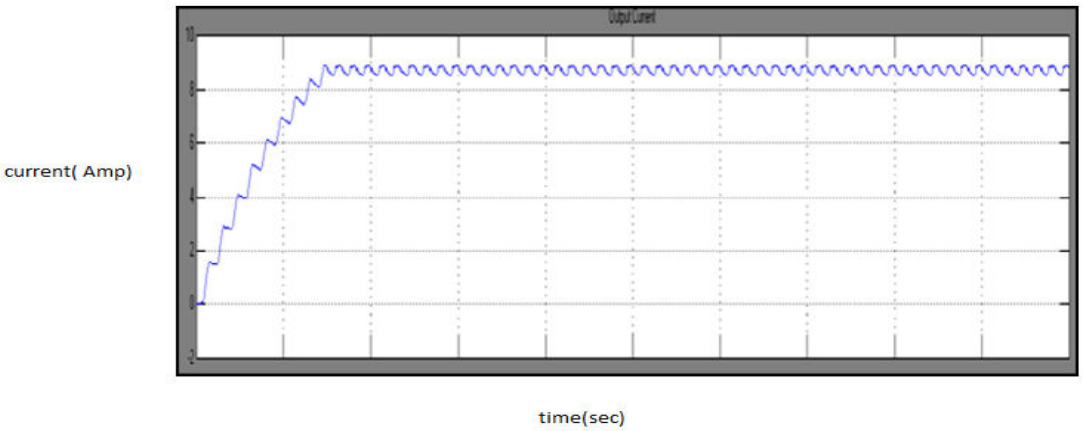


WAVEFORM OF INPUT CURRENT

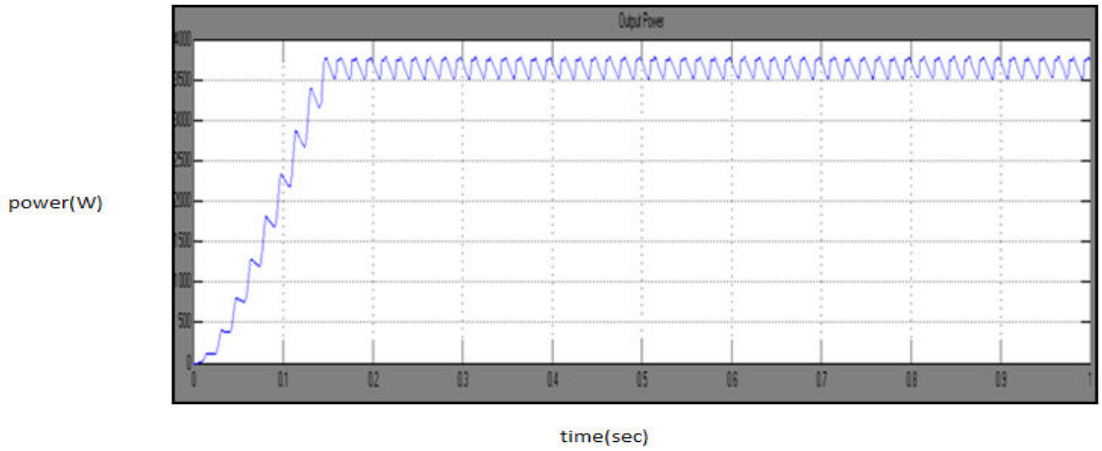
SIMULATION OUTPUT WAVEFORM



WAVEFORM OF OUTPUT VOLTAGE



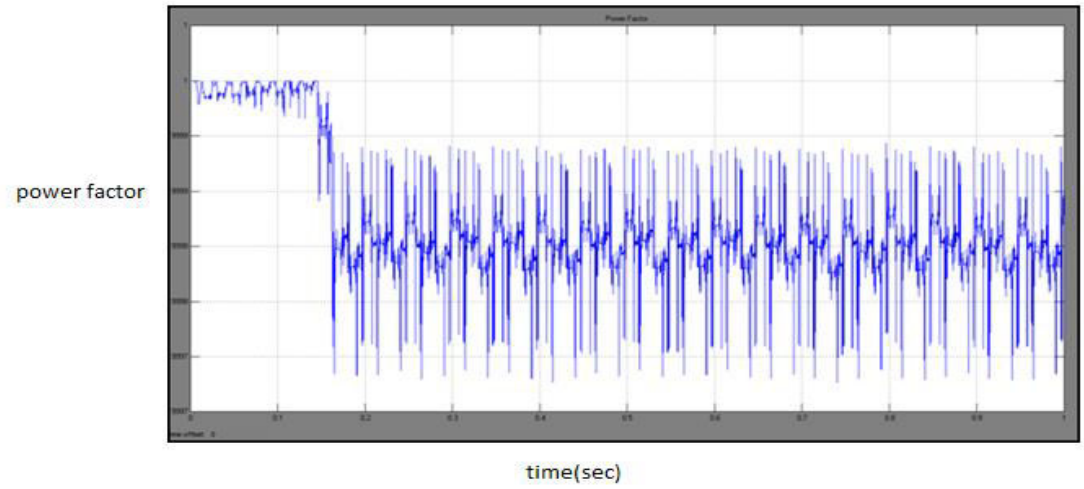
WAVEFORM OF OUTPUT CURRENT



WAVEFORM OF OUTPUT POWER

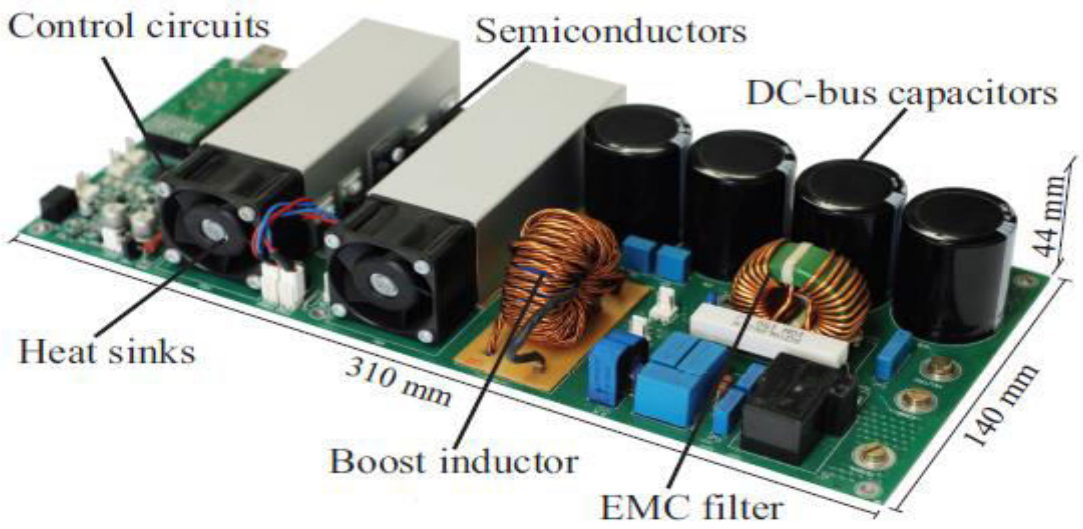
Using MATLAB Simulink the output voltage, output current and output power is obtained. Here from the output voltage waveform it is found that the output voltage is higher than the input voltage because of the usage of Boost converter. From the output waveform it is also found that the harmonics are reduced with the usage of multi-level converter compared to a two-level system .i.e., with the increase in the level the harmonics in the output tends to be reduced.

The power factor waveform is also obtained where it is nearly unity. In this case the switching losses and conduction losses are reduced. Here as multilevel converter is employed the efficiency tends to be higher.



WAVEFORM OF POWER FACTOR

HARDWARE MODEL OF PROPOSED SYSTEM



CONCLUSION

Multilevel high efficiency unidirectional single-phase PFC rectifier topologies well-suited for applications aiming for high efficiency and/or high power density have been proposed in this work. Thus, the proposed concepts present low switching losses when compared to conventional two-level bridgeless rectifiers. In addition, a simple to manufacture and small volume are characteristics of the required boost inductor. This leads to manufacturing cost advantages when comparing the proposed systems to interleaved converters. More importantly, the new converters feature similar switching loss performance, but lower conduction losses when compared to state-of-the-art three-level rectifier topologies. The selected circuit topologies enable very high efficiencies as a result of the excellent conduction and switching characteristics. Soft-switching concepts are thus not necessary and would also not be accepted by industry due to the increase in complexity resulting from the auxiliary circuit branches with additional losses and due to the typically complex state sequence within a switching period. In terms of system complexity, it should be noted that the restriction to unidirectional power flow does not allow a reduction e.g. a halving of the number of active semiconductors or a simpler control scheme. However, as the switching frequency rises, the efficiency of the three-level bridgeless is not as affected. This would be more pronounced if the boost inductor and EMC filter elements were considered. The voltages across the MOSFETs are presented where it is noted that all commutations occur with a voltage level equivalent to half the output voltage, even at the switches that need to block the full dc-link voltage. This produces low switching losses. Hence this multi-level concept is a very promising PFC solution due to lower conduction losses, and the lower number of diodes and gate driver potentials.

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