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DEVELOPMENT OF DC SOURCE BASED SYSTEM GENERATOR USING SPWM FOR HIGH SWITCHING FREQUENCY DC/AC INVERTERS

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ABSTRACT

The digital implementations of Sinusoidal Pulse Width Modulation (SPWM) generators have dominated over their counterparts based on analog circuits. In this paper, an FPGA- based SPWM generator is presented, which is capable to operate at switching frequencies up to 1 MHz (requiring FPGA operation at 100–160 MHz), thus it is capable to support the high switching frequency requirements of modern single-phase dc/ac power converters. The proposed design occupies a small fraction of a medium-sized FPGA and, thus, can be incorporated in larger designs. The post layout simulation and experimental results confirm that compared to the past-proposed SPWM generation designs, the SPWM generator presented in this paper exhibits much faster switching frequency, lower power consumption, and higher accuracy of generating the desired SPWM waveform. The digital SPWM generator implementations have dominated over their counterparts based on analog circuits, since they offer higher noise immunity and less susceptibility to voltage and temperature variations typically , microcontrollers, Digital Signal Processors (DSPs) or Field Programmable Gate Arrays (FPGAs) are used for the implementation of the SPWM generation unit and the execution of dc/ac inverter control algorithms.

Index terms: APWM, FPGA, DSP, SPWM.

I INTRODUCTION

The dc/ac converters (inverters) are the major power electronic conversion units in renewable energy production m o t o r drive, and uninterruptible power supply application. A simplified block diagram of a single-phase, full-bridge dc/ac power converter (inverter) is depicted. The Sinusoidal Pulse Width Modulation (SPWM) technique is widely employed in order to adjust the dc/ac inverter output voltage amplitude and frequency to the desired value. In this case, the power converter switches (e.g., MOSFETs, IGBTs, etc.) are set to the ON or OFF state according to the result of the comparison between a high-frequency, constant- amplitude triangular wave (carrier) with two low-frequency (e.g., 50 Hz).A low pass LC-, LCL- or LLCL type filter thus producing the high-power and low-frequency sinusoidal waveform Vo at the output terminals of the dc/ac inverter.

Moore's law affected the whole IC industry in terms of cost, speed, functionality, overall efficiency and reliability. Nowadays, fast and highly sophisticated IC's can be purchased with relatively low cost. Intel Corporation has already launched sophisticated microprocessors with diverse functions and high capabilities running in the GHz range (the latest Pentium IV microprocessor by Intel runs at 3 GHz). Furthermore, Intel is currently working on increasing the speed to tens of GHz in the near future. The growth in IC industry prompted the unprecedented advancement in the technology of Field Programming Gate Array which led to many commercial as well as residential applications and devices based solely on fast multi–functional digital microprocessors. The development path in semiconductor technology did not fail to follow the famous prediction of Moore's Law,

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stating that the number of transistors on a chip doubles about every two years. A clear impact of Moore's law can be noticed on the continuous increase of the number of transistors on processors and microprocessors. The benefits reaped out from applying Moore's law, specifically speaking on Microprocessors did not come free of remuneration; many design and control challenges paralleled the advantages discussed above. Explains the consequential downfalls faced by design engineers as a counterpart to the advantages of Moore's law by providing for dynamically scalable and often virtualized resources as a service over the Internet. To date, there are a number of notable commercial and individual cloud computing services, including Amazon, Google, Microsoft, Yahoo, and Sales force . Details of the services provided are abstracted from the users who no longer need to be experts of technology infrastructure. Moreover, users may not know the machines which actually process and host their data. While enjoying the convenience brought by this new technology, users also start worrying about losing control of their own data. The data processed on clouds are often outsourced, leading to a number of issues related to accountability, including the handling of personally identifiable information. Such fears are becoming a significant barrier to the wide adoption of cloud services . To allay users' concerns, it is essential to provide an effective mechanism for users to monitor the usage of their data in the cloud. For example, users need to be able to ensure that their data are handled according to the service level agreements made at the time they sign on for services in the cloud. Conventional access control approaches developed for closed domains such as databases and operating systems, or approaches using a centralized server in distributed environments, are not suitable, due to the following features characterizing cloud environments. First, data handling can be outsourced by the direct cloud service provider (CSP) to other entities in the cloud and theses entities can also delegate the tasks to others, and so on. Second, entities are allowed to join and leave the cloud in a flexible manner. As a result, data handling in the cloud goes through a complex and dynamic hierarchical service chain which does not exist in conventional environments. To overcome the above problems, we propose a novel approach, namely Cloud Information Accountability (CIA) framework, based on the notion of information accountability . Unlike privacy protection technologies which are built on the hide-it-or-lose-it perspective, information accountability focuses on keeping the data usage transparent and track able (as is proven by the popularity of Flicker and are increasingly hosted in the cloud as part of the storage services offered by the utility computing paradigm featured by cloud computing. Further, images often reveal social and personal habits of users, or are used for archiving important files from organizations. The SPWM pulse train is produced by comparing the sinusoidal and triangular signals generated according to the direct digital synthesis (DDS) technique. The comparison is performed using a high-speed analog comparator. The DDS approach is also used in for the development of a digital SPWM generator chip using 0.35-μm CMOS technology. The maximum clock frequency of this chip is 50 MHz. In the SPWM unit is composed of a DSP chip accomplishing the calculation of the widths of the individual pulses comprising the SPWM wave, which communicates through a parallel port with an FPGA-based unit producing the SPWM control signals.

II PROBLEM AND ANALYSIS

In this section, we first review related works addressing the privacy and security issues in the cloud. Then, we briefly discuss works which adopt similar techniques as our approach but serve for different purposes.

BIT-STREAM-BASED PWM TECHNIQUE FOR SINE WAVE GENERATION

The converter includes two full-bridge HF LCL-type resonant inverters working at fixed duty cycle. The power control is realized by means of the phase shift between the two bridges. generalized scalar pulse width modulation (PWM) approach, which unites the conventional PWM methods and most recently developed reduced common mode voltage PWM methods under one umbrella, is established. Through a detailed example, the procedure to generate the pulse patterns of these PWM methods via the generalized scalar PWM approach is illustrated. With this approach, it becomes an easy task to program the pulse patterns of various high performance PWM methods and benefit from their performance in modern three-phase, three wire voltage-source inverters for applications such as motor drives, PWM rectifiers, and active filters. The theory is verified by laboratory experiments. Easy and successful implementation of

various high-performance PWM methods is illustrated for a motor drive.

SINGLE PHASE INVERTER CONTROL TECHNIQUES FOR AN INTERFACING RENEWABLE ENERGY SOURCES WITH MICROGRID

A novel current control technique is proposed to control both active and reactive power flow from a renewable energy source feeding a micro grid system through a single-phase parallel-connected inverter. The parallel-connected inverter ensures active and reactive power flow from the grid with low-current total harmonic distortion even in the presence of nonlinear load. A p–q theory-based approach is used to find the reference current of the parallel-connected converter to ensure desired operating conditions at the grid terminal. The proposed current controller is simple to implement and gives superior performance over the conventional current controllers, such as rotating frame proportional–integral controller or stationary frame proportional resonant controller. The stability of the proposed controller is ensured by direct Lyapunov method. A new technique based on the spatial repetitive controller is also proposed to improve the performance of the current controller by estimating the grid and other periodic disturbances. Detailed experimental results are presented to show the efficacy of the proposed current control scheme along with the proposed nonlinear controller to control the active and reactive power flow in a single-phase micro grid under different operating conditions.

GRID CONVERTERS FOR PHOTOVOLTAIC AND WIND POWER SYSTEMS

Grid converters are the key player in renewable energy integration. The high penetration of renewable energy systems is calling for new more stringent grid requirements. As a consequence, the grid converters should be able to exhibit advanced functions like: dynamic control of active and reactive power, operation within a wide range of voltage and frequency, voltage ride-through capability, reactive current injection during faults, grid services support. This book explains the topologies, modulation and control of grid converters for both photovoltaic and wind power applications. In addition to power electronics, this book focuses on the specific applications in photovoltaic wind power systems where grid condition is an essential factor. With a review of the most recent grid requirements for photovoltaic and wind power systems, the book discusses these other relevant issues. A new technique based on the spatial repetitive controller is also proposed to improve the performance of the current controller by estimating the grid and other periodic disturbances. The bit streams, being binary in nature, can be interfaced to gate drivers with minimal conditioning. The nature of the implementation is concurrent or parallel, and hence, multiple instances of sinusoidal generators have no impact on each other. If required, the multiple generators can be synchronized to produce multiphase sinusoids with user-specified phase angle relationships. It is basically a digital form of the conventional analog duty cycle generation.

EXPERIMENTAL PERFORMANCES OF THE SINGLE-PHASE WAVE –MODULATED INVERTER

This paper presents the real-time implementation and experimental performances of the wavelet-modulation technique for single-phase voltage-source (VS) inverters. The wavelet-modulation technique is realized through constructing a non dyadic-type multi resolution analysis, which supports sampling of a sinusoidal reference-modulating signal in a non uniform recurrent manner, then reconstructing it using the inverter-switching actions. The required non uniform recurrent sampling is carried out by using dilated and translated sets of wavelet basis functions, which are generated by the scale-base linearly combined scaling function. The reconstruction of the sampled signal is accomplished by using dilated and translated sets of wavelet basis functions, which are generated by the scale-base linearly combined synthesis scaling function. The dilated and translated sets of wavelet basis functions used in the reconstruction are employed as switching signals to activate the inverter-switching elements. The wavelet-modulation technique is implemented in real time by using a digital signal processing board to generate switching pulses for a single-phase VS H- bridge (four-pulse) inverter. Experimental performances of the single-phase inverter, which is operated by the wavelet-modulation technique are investigated while supplying linear, dynamic, and nonlinear loads with different frequencies. Experimental test results show that high magnitude of fundamental components and significantly reduced harmonic contents of the inverter outputs can be achieved using the wavelet-modulation technique. The

efficiency of the developed modulation technique is further demonstrated through performance comparisons with the pulse width- and random-pulse width-modulation techniques for similar loading conditions.

GENERALIZED SCALAR PWM APPROACH WITH EASY IMPLEMENTATION FEATURES FOR THREE-PHASE, THREE-WIRE VOLTAGE-SOURCE INVERTER

The generalized scalar pulse width modulation (PWM) approach, which unites the conventional PWM methods and most recently developed reduced common mode voltage PWM methods under one umbrella, is established. Through a detailed example, the procedure to generate the pulse patterns of these PWM methods via the generalized scalar PWM approach is illustrated. With this approach, it becomes an easy task to program the pulse patterns of various high performance PWM methods and benefit from their performance in modern three-phase, three wire voltage-source inverters for applications such as motor drives, PWM rectifiers, and active filters. leading to a decrease in the total inductance and volume. Furthermore, by decreasing the inductance of a grid-side inductor, it raises the characteristic resonance frequency, which is beneficial to the inverter system control. The parameter design criteria of the proposed LLCL filter is also introduced. The theory is verified by laboratory experiments The PWM technique presented in , targets to reduce the amount of computation time required in order to facilitate the generation of higher switching frequencies online and in real time. In this technique, the pulse width is calculated once and used over *N* consecutive switching edges of the SPWM wave pulses. Then, a new sample of the reference sine wave is acquired. Thus, the sampling frequency f_S is reduced by an integer factor of *N*. The digital SPWM generator implementations have dominated over their counterparts based on analog circuits. Digital Signal Processors (DSPs) or Field Programmable Gate Arrays (FPGAs) are used for the implementation of the SPWM generation unit and the execution of dc/ac inverter control algorithms (e.g., output voltage regulation, fuzzy logic, motor speed control, etc.) . The integration of both the control and SPWM in the same chip has the advantage of reducing the design complexity and the total system cost . However, the microcontroller and DSP-based implementations of the SPWM generator units developed so far operate at low switching frequency levels (i.e., 1–10 kHz). The computational speed of microprocessors and DSPs imposes an upper limit on the maximum switching frequency that can be generated using software-based SPWM generation techniques. Easy and successful implementation of various high-performance PWM methods is illustrated for a motor drive.

PROBLEM STATEMENT

A phase-modulated high-frequency isolated DC/AC converter is proposed for a PMSG-based grid-connected wind generation application. The converter includes two full-bridge HF LCL-type resonant inverters working at fixed duty cycle. The power control is realized by means of the phase shift between the two bridges. With the LCL-type resonant tank, zero-voltage-switching is achieved for all switches for the whole power range. With the phase shift modulated sinusoidal, a 120 Hz rectified output current is obtained, which is unfolded and fed to the single-phase utility line. leading to a decrease in the total inductance and volume. Furthermore, by decreasing the inductance of a grid-side inductor, it raises the characteristic resonance frequency, which is beneficial to the inverter system control. The parameter design criteria of the proposed LLCL filter is also introduced. The analysis is verified with computer simulation results. The digitally controlled switching converter. The resultant error signal is subsequently minimized through the action of a compensator that generates a duty cycle command.

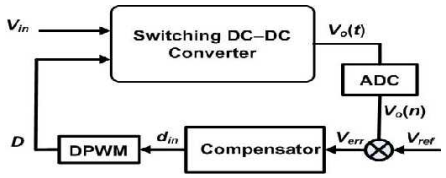


Figure 1 Digitally Controlled DC–DC Buck Converter

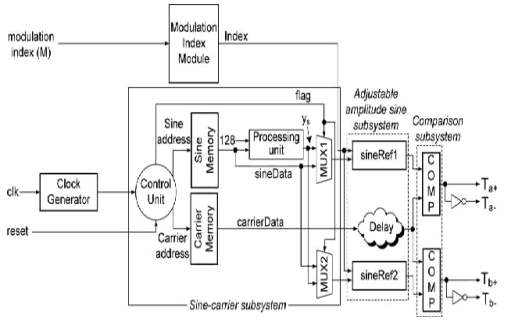
The compensator is designed to maintain a near zero error signal during steady–state and to enhance the dynamic performance during transients. The DPWM unit translates the duty cycle command of the compensator, to an analog driving signal, controlling the ON–time of the switching Converter. Consequently, a well designed PID compensator and high resolution DPWM architecture are essential to achieve a tightly regulated converter. Experimental data based on a 500 W prototype circuit is included for validation purpose. single-phase voltage-source (VS) inverters. The

wavelet-modulation technique is realized through constructing a non dyadic-type multi resolution analysis, which supports sampling of a sinusoidal reference- modulating signal in a non uniform recurrent manner, then reconstructing it using the inverter-switching actions. The simplest DPWM architecture is a direct emulation of the PWM ramp, offering the best linearity. It is basically a digital form of the conventional analog duty cycle generation where a digital saw–tooth signal with a frequency equals to the switching frequency of the converter, is compared to the duty cycle value coming from the compensator, The duty cycle is set high every time the counter of the ramp signal resets to zero. On the other hand, the comparator resets the duty cycle by triggering the instance at which the commanded duty cycle exceeds the ramp signal. The DPWM and the switching frequency determine the clock frequency of the counter. Hence, with Low switching frequencies and Low DPWM resolution, the required clock frequency may be impractically large, particularly in terms of power consumption. The bit streams, being binary in nature, can be interfaced to gate drivers with minimal conditioning. The nature of the implementation is concurrent or parallel, and hence, multiple instances of sinusoidal generators have no impact on each other. If required, the multiple generators can be synchronized to produce multiphase sinusoids with user-specified phase angle relationships. The digital circuits have been simulated using very high speed integrated circuits hardware description language (VHDL) within modelsim and synthesized on a Static field-programmable gate array (FPGA) using Altera's Quartus tool chain. The power circuits have been designed and constructed in-house. The DPWM and the switching frequency determine the clock frequency of the counter. The system inputs are the modulation index of the output SPWM wave M in single precision floating point arithmetic ranging from 0 to 1, as well as the "clock" and "reset" signals. The architecture of the proposed system has been built using 8-bit fixed-point arithmetic and it consists of five subsystems, which implement the SPWM generation algorithm. The values of a sinusoidal wave, mathematically being in the range [−1,1], have been adapted in the proposed architecture to the equivalent range of [0, 255] with the zero point corresponding to the discrete value of "128." The digital SPWM generator implementations have dominated over their counterparts based on analog circuits, since they offer higher noise immunity and less susceptibility to voltage and temperature variation. Typically, microcontrollers, Digital Signal Processors (DSPs) or Field Programmable Gate Arrays (FPGAs) are used for the implementation of the SPWM generation unit and the execution of dc/ac inverter control algorithms (e.g., output voltage regulation, fuzzy logic, motor speed control, etc.). The integration of both the control and SPWM subsystems in the same chip has the advantage of reducing the design complexity and the total system.

Architecture Of SPWM Generation Unit

In SPWM pulse train is produced by comparing the sinusoidal and triangular signals generated according to the direct digital synthesis (DDS) technique. The comparison is performed using a high-speed analog comparator. The DDS approach is also used for the development of a digital SPWM generator chip using 0.35-μm CMOS technology. The maximum clock frequency of this chip is 50 MHz. In the SPWM unit is composed of a DSP chip accomplishing the calculation of the widths of the individual pulses comprising the SPWM wave, which communicates through a parallel port with an FPGA-based unit producing the SPWM control signals. The regular- sampled PWM technique presented , targets to reduce the amount of computation time required in order to facilitate the generation of higher switching frequencies online and in real time. In this technique, the pulse width is calculated once and used over N consecutive switching edges of the SPWM wave pulses. Then, a new sample of the reference sine wave is acquired. It was an inefficient scheme of PWM can be used to reduce the total amount of power delivered to a load without losses normally incurred when a power source is limited by resistive means. This is because the average power delivered is proportional to the modulation duty cycle. Using pulse width modulation (PWM) in power electronics control system is there are different approaches for developing pulse width modulation. Many digital circuits can generate PWM signals, but what is interesting is, to generate pulse width modulation using Hardware Description Language (VHDL) and implementing it in FPGA. Pulse width modulation (PWM) is a technique to provide a logic "1" and logic "0" for a controlled period of time. It is a signal source involves the modulation of its duty cycle to control the amount of power sent to a load. The following sections describe the design of Pulse Width Modulation (PWM) on a

Xilinx FPGA using very high speed integrated circuit hardware description language (VHDL). The insufficient resolution obtained in digital pulse width modulators (DPWMs) has been one of the main obstacles to the expansion of digital control in the field of switching-mode power supplies. DPWM resolution Is a problem mainly for two reasons. The PV voltage is regulated instantaneously to the command generated by the MPPT function block. High bandwidth proportional-integral control is adopted to track the voltage reference and to minimize double line-frequency disturbance from LVS dc link. The capacitor voltage differential feedback is introduced for active damping of the input LC resonance. Typically, the MPPT function block in a PV converter/inverter system periodically modifies the tracking reference of the PV voltage, or the PV current. In most cases, these periodic perturbations yield step change dynamic responses in power converters. The vC1–vC4 is changing dynamically in accordance with d1. As a result, at any time, the charge and discharge rate of C1-C4 must be limited such that the transformer flux is not saturated. For the sake of control simplicity and low cost, developing a customized MPPT method by carefully taking care of the boost-half- bridge converter dynamics. The first one is that high DPWM resolution is needed in order to avoid limit cycling. Thus, the sampling frequency is reduced by an integer factor of N , resulting in the following relationship with the corresponding carrier frequency Consequently, the number of calculations required to produce the complete SPWM waveform is N times less than in the conventional SPWM generation methods. The proposed design exhibits architectural flexibility features, enabling the change of the SPWM switching frequency and modulation index either internally, or externally. The proposed SPWM unit has been implemented in a single chip in order to enable the reduction of the complexity, cost, and development time of the dc/ac inverter control unit.



A common disadvantage of the previously proposed SPWM generators described previously is that they have been designed to operate at low-switching frequencies (i.e., 1–20 kHz), while their operation at higher switching frequencies has not been explored yet. In this paper, an FPGA-based SPWM generator is presented, which is capable to operate at switching frequencies up to 1 MHz; thus, it is capable to support the high switching frequency requirements of modern single-phase dc/ac power converters. Compared to the past-proposed SPWM generators, in the proposed architecture the values of both the reference sine and triangular waves are stored in the FPGA de-vice Block RAMs (BRAMs) in order to exploit their one-clock- cycle access time, thus providing a much higher switching-frequency capability.

CLOCK GENERATOR SUBSYSTEM

The "Clock generator" subsystem takes as input the FPGA input clock and produces a new clock signal used by the digital circuits of the proposed SPWM generator, such that the desired SPWM switching frequency fc specified by the designer/user is generated. A two-state finite state machine (FSM) is initially used to set the input clock frequency fclk to fclk /2 and then a Digital Clock Manager module adapts this frequency to the desired value. The Very high speed integrated circuit Hardware Description Language (VHDL) code of the DCM module is illustrated in Fig. 5. The FSM is kept constant for every different switching frequency, while only the operational parameters "CLKFX_MULTIPLY" and "CLKFX_DIVIDE" of the DCM module are changed according to the switching frequency requirements of the SPWM output waveform. Thus, the proposed SPWM generator is flexible to be adapted to the generation of any operating switching frequency specified by the system designer/user.

MODULATION INDEX SUBSYSTEM

The "Modulation index" subsystem is used to convert the floating-point modulation index M , which is input in the pro- posed SPWM generation system [0, 1]) to the corresponding value in fixed-point arithmetic. Increasing the value of n enables to control the modulation index of the generated SPWM wave with higher resolution, but also results in higher requirements for FPGA device re- sources. The floating point value produced is then converted into a fixed-point value ranging from 0 to 255, via a float-to-

fixed point conversion unit, thus producing the "Index" output of the "Modulation index" subsystem.

SINE-CARRIER SUBSYSTEM

The "Sine-Carrier" subsystem consists of the control unit, two BRAMs, which contain samples of the sinusoidal and tri-angular(i.e., carrier) waves and two multiplexers that produce the two constant-amplitude reference sine waves used for the production of the SPWM output signals.

ADJUSTABLE AMPLITUDE SINE SUBSYSTEM

The "Adjustable amplitude sine" subsystem takes as input the constant- amplitude reference sinusoidal values produced by the "Sine-Carrier" subsystem and generates a sinusoidal digital signal ya with an amplitude adjustable according to the value of the modulation index M which is an input in the proposed SPWM generation system.

III MECHANISM AND SOLUTION

In this section, we first introduce the settings of the test environment and then present the performance study of our system.

EXPERIMENTAL RESULTS

A laboratory prototype of the proposed FPGA-based SPWM generation system was implemented using the commercially available XILINX XUPV5-LX110T development board for downloading the implemented SPWM design, which contains the XC5VLX110T Virtex-5FPGA device. The pro- posed SPWM generator is suitable for incorporation in single- phase dc/ac inverter applications and as an example, the experimental, oscilloscope measurements of the T_a + SPWM control signal (T_a –, T_b + , and T_b – exhibit similar patterns) in case that f_c = 1 kHz and f_c = 1 MHz. Using a 1-MHz carrier frequency, results in 20 000 pulses spread over the 1/50 Hz time period of the T_a + signal. Thus, in order to enable the visibility of the individual SPWM pulses, two different portions of this signal are illustrated separately in the upper and lower waveforms, respectively. Then, a unity-gain differential amplifier was used in order to subtract the T_a + and T_b + control signals generated by the pro- posed SPWM generation system (see Fig. 2), thus producing a wave equivalent to the output SPWM signal of a single-phase dc/ac inverter, $V_{\mathrm{spw\,m}}$ in Figs. 1 and 2. This hardware-emulation process has the advantage of low cost, since building an actual power stage of a single-phase dc/ac inverter (including power switches, drivers, etc.) is avoided. It enables to evaluate the performance of the proposed SPWM genera- tor without being affected by non idealities of an experimental prototype dc/ac power inverter (e.g., dead-time effect, power switch finite turn-on, and turn-off times, etc.), which depend on the exact type of the dc/ac inverter application comprising the proposed SPWM generator and deteriorate the quality of the generated SPWM signal . The minimization of the impact of such effects is performed during the design process of the dc/ac inverter; thus, the investigation of their impact on the quality of the SPWM output voltage of the dc/ac inverter is not within the scope of this paper. The hardware-emulation process described previously has been applied in order to experimentally evaluate the performance of both the new SPWM generator presented in this paper, as well as that of the past-proposed SPWM generation units.

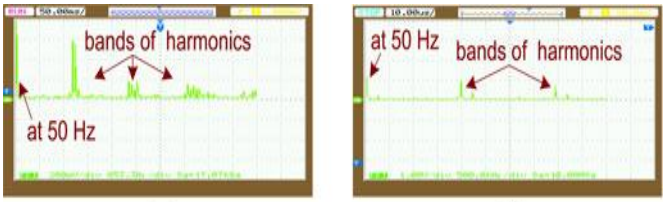
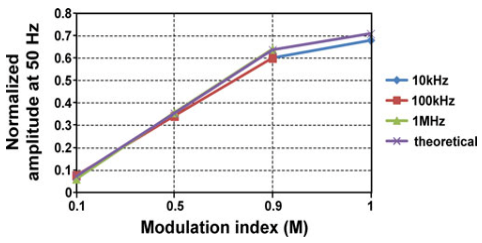


Fig 1. FFT of the experimentally measured unipolar SPWM output waveform for single-phase applications: (a) f_c = 1 kHz, f_s = 4 MHz, and M = 0.9 and (b) f_c = 1 MHz, f_s = 32 MHz, and M = 0.5.

The Fast Fourier Transforms (FFTs) of the experimentally measured SPWM output waveforms, which are produced by the hardware emulation process described previously, in case that the SPWM switching frequency f_c is 1 kHz and 1 MHz . It is observed that, as expected due to the attributes of the unipolar SPWM technique, the generated SPWM signal consists of the fundamental at 50 Hz, while the harmonics appear as sidebands at multiples of twice the switching frequency.



A post place-and-route analysis of the implemented system has been performed using the XILINX ISE Design Suite 10.1 software. The dynamic, quiescent, and total power consumption of the FPGA device in the post place-and-route implementation of the proposed system have been derived using the power analyzer of the XILINX ISE Design Suite 10.1 software and they are plotted in Fig. 11 as a function of f_C / f_S . The total power consumption at the 1 / 64 MHz upper end is 6.1% higher compared to that at 10 kHz/4 MHz. The BRAMs of the sine wave and carrier operate as LUTs. Both the sinusoidal and triangular waves are sampled and quantized with the same sampling frequency fs using MATLAB (e.g., fs = 4, 8 MHz, etc.). In order to minimize the utilization of the FPGA resources, only the values of the first quarter of the constant-amplitude sine-wave period (i.e., during the time interval $0-\pi/2$) are stored in the corresponding BRAM, while the values of the sine wave during the time interval $\pi/2 - 2\pi$ are calculated by mirroring and inverting the values of the first quarter. The presents A Novel Grid-Connected boost half- Bridge Photovoltaic (PV) Micro inverter System and Its Control Implementations. In Order To Achieve Low Cost, Easy Control, High Efficiency, And High Reliability, A Boost- Half-Bridge Dc–Dc Converter Using minimal Devices Is Introduced To Interface The Low-Voltage PV Module. A Full-Bridge Pulse width-Modulated Inverter Is Cascaded And Injects Synchronized Sinusoidal Current To The Grid. Moreover, A Plug-In Repetitive Current Controller Based on a Fourth-Order Linear phase IIR Filter Is Proposed To Regulate The Grid Current. High Power Factor And Very Low Total Harmonic Distortions Are Guaranteed Under Both Heavy Load And Light Load Conditions. Dynamic Stiffness Is Achieved When Load Or Solar Irradiance Is Changing Rapidly. In Addition, The Dynamic Behavior Of The Boost-Half-Bridge Dc–Dc Converter Is Analyzed; A Customized Maximum Power Point Tracking (MPPT) Method, Which Generates A Ramp-Changed PV Voltage. Variable Step Size Is Adopted Such That Fast Tracking Speed And High MPPT Efficiency Are Both Obtained. A 210W Prototype Was Fabricated And Tested. The BRAM of the carrier contains the values of a complete period of the reference triangular wave. Depending on the values of f_C and f_S , 97.04–98.43% of the total power consumption corresponds to the quiescent power, while the rest is consumed during dynamic operating conditions. The resources required for the implementation of the full system are presented in Table I for various combinations of the sampling and carrier frequencies f_S and f_C respectively. The corresponding maximum operating clock frequency values are shown in the last row of Table I. It is observed that the proposed design is capable to operate at switching frequency values up to 1 MHz, thus covering the requirements of modern single-phase dc/ac power converters. Also, a low percentage of the FPGA device logic and memory blocks are occupied by the proposed SPWM generation architecture enabling the implementation of additional dc/ac inverter control algorithms in the same FPGA IC (e.g., for regulating the dc/ac inverter output voltage, current or frequency to the desired value, etc.). Increasing the sampling frequency f_S results in a more accurate calculation of the widths of the individual SPWM pulses, but, as shown in Table I, the BRAM memory requirements for the LUTs for the sinusoidal and carrier waves are also increased. Additional tests performed for higher sampling frequencies indicated that the BRAMs are the critical resource that restricts further increase of the sampling frequency (e.g., to 128, 256 MHz, etc.).

IV CONCLUSION

We proposed innovative approaches for automatically The previous Reference paper survey converter switching problem overcome the base paper sinusoidal pulse width modulation (SPWM) switching frequency 1Khz for High switching Speed generate converter or inverter operation. The modelsim software using memory unit generates the sine signal and carrier signal is produce SPWM signal Duty cycle based ON-OFF control the MOSFET switches in the voltage source inverter can be turned on and off as required. In the simplest approach the top switch is turned on if turned on and off only once in each cycle, a square wave waveform results using VHDL. A novel grid-connected Mosfets control the switching frequency 1 KHz fuse the system Generator using SPWM Signal convert the photovoltaic (PV) inverter system and its control implementations. MATLAB Simulation model for reduce the harmonic components are merely shifted into the higher frequency range and are automatically filtered due to inductances in the ac system. In terms of the FPGA resources required, all SPWM genera- tor architectures occupy a small fraction (≈9%) of the medium- sized FPGA device used. The BRAMs are the critical resource that restricts further increase of the

sampling frequency of the SPWM generator proposed in this paper. The next critical resources are the DSPs that occupy 3% more space in the FPGA device of the proposed SPWM generator. The SPWM principle is widely used in dc/ac inverters in energy conversion and motor drive applications. The past- proposed SPWM generators have been designed to operate at low switching frequencies (i.e., 1–20 kHz), while their operation at higher switching frequencies had not been explored so far. In this paper, an FPGA-based SPWM generator has been presented, which is capable to operate at switching frequencies up to 1 MHz, thus it is able to support the high switching frequency requirements of modern single-phase dc/ac inverters. The proposed design occupies a small fraction of a medium- sized FPGA and, thus, can be incorporated in larger designs, while it has a flexible architecture can be adapted to a variety of single-phase dc/ac inverter applications. Both post place and route simulation results and experimental results on actual hardware were presented, demonstrating the successful operation of the proposed SPWM generator at high switching frequencies. The past-proposed SPWM generation techniques were also implemented and their performance was compared to that of the new architecture presented in this paper. The post layout simulation and experimental results confirm that the proposed SPWM generator exhibits much faster switching frequency, lower power consumption, and higher accuracy of generating the desired SPWM waveform.

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