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# A new inductorless RGC lna design in 32 –nm CMOS technology

**Edamadaka Keerthana[1], P.Geerthana[1], R.S.Haritha[1], N.Ganesh[1], Dr.M.Anto bennet[2]**

[1]UG students, [2]Professor&HOD, Department of ECE Vel tech, Chennai-600062

## ABSTRACT

Research in optical communications has increased in importance as the necessity for greater data rates increased. The front-ended optical receiver plays a vital role in influential dynamic range, bandwidth and sensitivity for the complete network. Growth of demands for communication and advances in electronic devices, have nowadays lead to manufacturing high-speed communication systems. These high speed communication systems use a ray of light source to transfer massive volumes of data. At far-end the modulated data on a grin of light source is weakened and therefore to facilitate look up the quality of the received signal which is intended to be second-hand in digital circuits, the signal essentials to be appropriately amplified. The amplification process in CMOS analog circuits is a multi-objective design problem outstanding to the trade-off among gain bandwidth noise-power consumption and voltage headroom of the circuit which make the designer to confront difficulties and challenges in sub-micron CMOS equipment is used. A broadband CMOS LNA with pre-distortion method is projected in this project. The most essential for this project is to intend a linearization technique called pre-distortion to get better linearity with higher power efficiency. The proposed technique condenses the signal distortion and results in high linearity. This proposed intend is implemented in 32-nm CMOS technology and aims at achieving linearity of IIP3. This complete setup is being designed by using Tanner EDA v.16.0 toolkit.

**Keywords:** Limiting Amplifier (LA), System-on-a-chip (SoC),Complementary Metal-Oxide Semiconductor (CMOS) technology.

## INTRODUCTION

Research in optical communications has increased in importance as the necessity for greater data rates increased. The front-ended optical receiver plays a vital role in influential dynamic range, bandwidth and sensitivity for the complete network. The front ended optical receiver contains the photodiode, TIA and Limiting Amplifier (LA).To achieve high voltage gain in CMOS process whereas existing .circuit provides gain in CMOS process and adequate input matching and maintaining small power consumption. To obtain elevated linearity is to minimize tradeoff between voltage gain & input impedance. To implement the design in CMOS technology with the good LNA's performance with the high frequency of operation. The foremost rapid digital communication standard at present is SONET OC-192 by 10 Gb/s being imperative [1].Firstly, the short-reach in the 10 Gb/s data communication values devour less inflexible optical sensitivity necessities versus those of long-haul principles. Secondly, 10 Gb/s silicon photo detectors are well-matched to the cheap 850 nm wavelength upright Cavity Surface Emitting Lasers (VCSEL) widely used for optical communication purpose .Although multi-order RC ladder networks or inter-stage inductive peaking can be used to increase bandwidth, reflected inductor less techniques because on-chip spiral inductors require huge amount of area, power and higher crosstalk resulting in performance degradation. Growth of demands for communication and advances in electronic devices,

**Author for correspondence:**
Department of ECE Vel tech, Chennai-600062

have nowadays lead to manufacturing high-speed communication systems. These high speed communication systems use a ray of light source to transfer massive volumes of data[2]. At far-end the modulated data on a grin of light source is weakened and therefore to facilitate look up the quality of the received signal which is intended to be second-hand in digital circuits, the signal essentials to be appropriately amplified. The amplification process in CMOS analog circuits is a multi- objective design problem outstanding to the trade-off among gain bandwidth noise-power consumption and voltage headroom of the circuit which make the designer to confront difficulties and challenges in sub-micron CMOS equipment is used. Z gain of 26.88dB and NF of 2.55dB and the Differential LNA exhibits a gain of32.71dB and Noise Figure of 2.66dB. The circuits are designed using TANNER 0.035µmRF CMOS technology[3]. The traffic of audio and video based messages has grown in recent years. Which led to the need for even gradually higher data-rates for the next generation wireless communication applications. The cellular telephony and wireless local area networks (WLANs) are the two prime directions and in recent years, realization of fully integrated system-on-a-chip (SoC) has become a major interest in receiver front end design architectures while retaining low cost. This is the main reason for the Complementary Metal-Oxide Semiconductor (CMOS) technology to be very popular in RF circuit designs The interest has grown towards technologies which can offer higher data rates in large global areas A significant amount of research work has been done at 2.5GHz, because of its widespread global usage. Though, not much amount of work is stated in research or industrial for 3.5GHz, though it is much needed spectrum in many other uses, especially for the reason of the authorizing requirements. The focus is on very low cost communication to nearby devices without less power consumption and small underlying infrastructure. The LNA also used in W-CDMA applications at 3.5GHz[4,5].

## PROPOSED SYSTEM

A Broadband CMOS LNA with predistortion technique is proposed in this work. The main mean of this work is to propose a linearization technique called predistortion to get better linearity with higher power efficiency. The proposed technique reduces signal distortion and outcome is high linearity. This projected design is implemented on 90-nm CMOS technology and aims at achieving linearity of IIP3 greater than +14.3dbm. The predistortion is the linearization method proposed in LNA for high linearity. Predistortion compensate the nonlinearities in LNA. This predistortion technique minimizes the frequency interfering and signal distortion and allows superior transmission capacity in broadband communication systems. Linearization technique will allow LNA to have both high linearity and higher power efficiency. Predistortion is one on generic terms added to the technique which seeks to linearize the short noise amplifier by making the suitable modifications to the amplitude and phase of i/p signal. The predistortion branch is inserted at the front of the main device so as to cancel the bury modulation distortion of major device . The main key feature of this technique improves linearity in the broad range of i/p power without significant gain and noise figure degradation.

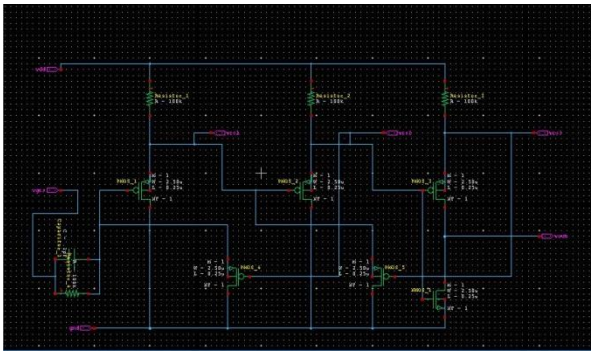

***Fig.1*.LNA Implementation circuit**

LNA are low noise, high gain, and high linearity. To achieve these goals simultaneously, a 2-stage topology is used where the first stage is optimized for lownoise and high-gain operation, whereas the second stage aims for high linearity and a high 1dB compression point using negative feedback. The first stage is using a cascade topology, which provides high gain andexcellent reverse isolation. Its noise figure has been optimized by proper biasing and noise matching shown in fig 1.

## IMPLEMENTATION OF PREDISTORTION TECHNIQUE

The proposed design of low noise amplifier employs a technique called Pre- distortion which suppress the inter modulation distortion in the low noise amplifier shown in fig 2.

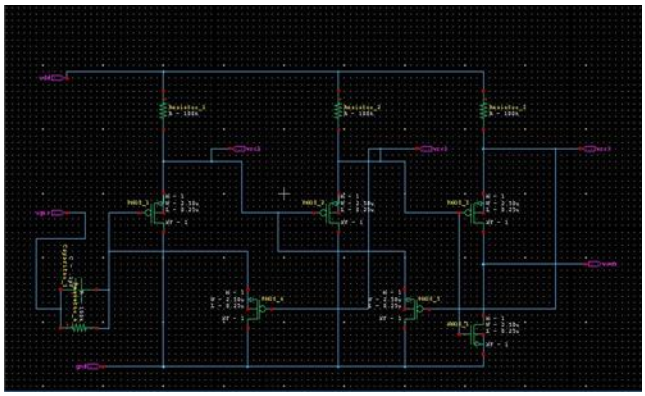

***Fig.2*.Predistortion Circuit**

## EXPERIMENTAL RESULTS

In this we will be building a low-noise preamplifier for the front end of your FM receiver. The input to this amplifier will be signals from an antenna, which we will model as a voltage source with a 50Ω source impedance. Although this may sound like a straightforward task, there are a number of complicating issues involved with processing a low-power, high frequency signal that we must keep in mind. These issues - noise, bandwidth, gain, and impedance matching - will apply to our entire transceiver system, but for now we shall frame them in the context of designing our low-noise amplifier shown in fig 3&4.

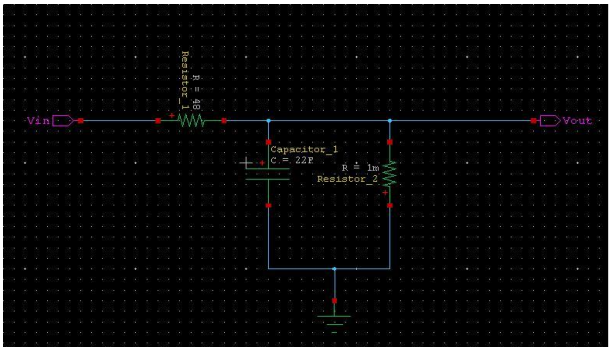


***Fig 3*. TIA Schematic Diagram**

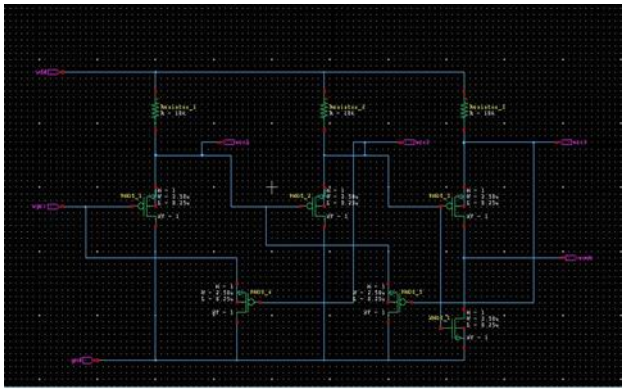

***Fig 4*. LNA Schematic Diagram**

## CONCLUSION

In conclusion a new inductor less RGC LNA design is shown in 32-nm CMOS technology ,which gives a good FOM tradeoff between gain ,bandwidth and power consumption on behalf of 10 Gb/s optical communication as shown in Table 1.2, is less affected by input capacitance and is expected to take up a very small extent of chip space is used to lower input impedance through cascade and parallel PMOS transistor techniques aimed at wideband operations .The amplifier stage used common source amplifiers to increase the gain and the third order interleaving feedback technique to increase the bandwidth and power consumption will be reduced upto 30~40% normally. And high amount of transmission rate is possible.

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