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Low power consumption of current mirrored footed domino comparator using lector technique

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ABSTRACT

This paper presents plan of a leakage-tolerant design technique for high fan-in dynamic circuits is presented. Diode Footed Domino (DFD) comparator is utilizing footer transistor in diode configuration to reduce sub threshold leakage. The power is not diminished by the use of comparator. Dynamic comparator is aimed by the diode footed domino method to exhibit the effectiveness of the wished-for structure in enlightening leakage-tolerant. A method using lector technique is proposed to reduce power. Lector is a technique to reduce the problem of leakage in CMOS circuits, it includes a n-type and p-type leakage controlled transistors (LCTs), between supply to ground which are self-controlled and proposals the additional resistance, which will diminish the difficult of leakage current in the CMOS circuits. LCT's is self-controlled transistors.

Index Terms: Diode footed domino, Lector, Domino logic, CMOS, Comparator, Power consumption.

INTRODUCTION

VLSI stands for Very Large Scale Integration which is used in designing or manufacturing of extremely small complex circuitry using modified semiconductor material. The main advantage of using VLSI is that systems are much smaller and consume less power than the discrete components used to build electronic systems. Logic maneuvers within a chip as well take ample not as much of power. Once over again, lower power consumption is mostly due to the slight dimension of circuits on the chip-smaller parasitic capacitances and resistances necessitate less power to drive them. Dynamic circuits are the circuits whose yield is preferred by accusing and discharging of capacitor at the yield. That one integrates a precharge circuit and an resultant circuit for precharging dynamic nucleus and possession dynamic nucleus at its current voltage level. It can as well integrate a detachment transistor coupled among the dynamic nucleus and the yield nucleus [1]. The Complementary Metal Oxide Semiconductor (CMOS) in progress to develop the procedure of select for digital semiconductor designs. CMOS logic gates dissipate almost low power when the inputs to the gate do not change. This tails as CMOS holds both PMOS Field Effect Transistors (FETs), which can effectually drive a high voltage, or logic one value, and NMOS transistors, which are worthy at driving a zero voltage [2]. CMOS logic dissolves less power than NMOS logic circuits for the reason that CMOS dissolves power only when converting ("dynamic power"). NMOS logic dissolves power at whatever time the transistor in on, for there is a current footpath from VDD to VSS through the load resistor and the n-type network. CMOS gates are very power efficient because they dissipate nearly zero power when idle [3].

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POWER DISSIPATION

Idyllically, in steady state of CMOS circuits there is not one static power dissipation, then this is the most gorgeous individualities of CMOS technology. It is a type of dissipation, which does not have any effect of level change in the input and output. That is the power dissipation occurring when device is in standby mode [4]. The main causes of static power dissipation are listed below,

1. Sub threshold conduction when the transistors are OFF
2. Tunneling current through gate oxide
3. Leakage current through reverse biased diodes

Dynamic switching power as well as short circuit power are active elements of power dissipation. These occur due to transitions at gate terminals which are caused by charging and discharging of capacitors in the circuit [5]. In the proposed circuit, the manager proportion is kept as low as conceivable to have a superior speed and power execution.

The power utilization in a rationale door [6] is given by

Pavg/gate = Pswitching + Pshort−circuit + Pleakage (1)

Where,

- Pswitching is the power utilization by charging and releasing of the capacitances offered by circuit transistors,
- Pshort−circuit is the power utilization caused because of direct association of VDD to the ground even though yield switching,
- Pleakage is the power consumption because of several spillage movements in the MOS gadgets.

The term Pswitching clarified above is given by [7] as,

Pswitching = α0→1CLVDDVswingf (2)

Where α0→1 is the possibility of moving yield from low to high for each clock cycle named exchanging movement, f is the most extreme recurrence of the data sources together with clock flag, CL is the heap capacitance and Vswing is the greatest yield voltage swing of the rationale circuit.

Few exploration groups have technologically advanced power replicas for the approximation of leakage power dissipation. However, most of this model are at a transistor level, and are not feasible for efficient architecture power dissipation simulation. Even though approximation may be suitable with current process parameters, well leakage power estimation should be combined into power estimation tools. The model of leakage power as:

$$P_{leakage} = V_{dd} N K_{design} I_{leak} \quad (3)$$

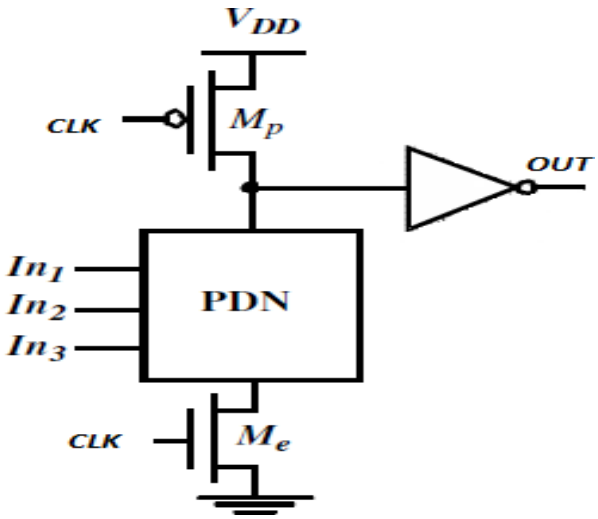

Figure 1: Domino logic

Where,

- $P_{leakage}$ is the static power consumption at the architectural level,
- N is the number of transistors,
- K_{design} is a design dependent parameter,
- I_{leak} is a technology dependent parameter like V_{th} while K design.

A domino logic module consists of an N-type dynamic logic block followed by inverter. Figure 1 shows the general diagram of domino logic. For the duration of precharge, the output of the N – type dynamic gate is stimulating up to VDD and the output of the inverter is fixed to 0. During evaluation, the dynamic gate conditionally discharges, and the output of the inverter makes a conditional transition from 0→1.The introduction of static inverter has additional advantage that the fan-out of the gate is driven by a static inverter with low impedance output with increases noise immunity.

LITERATURE REVIEW

Now we good graces sometime years, major part of the cardinal boundary deep-laid is done using impetuous reasonability resulting among other things well-rounded probing work in this field. Discussion with respect to accomplished refer to the domino techniques are give details inside of this section.

Domino circuits are broadly used in high-speed uses for the putting into practice of high fan-in circuits. However, domino circuits are vulnerable to noise. The noise consideration of domino circuits is due to their short switching threshold voltage, which is the similar to threshold voltage of NMOS devices in the evaluation process. The substantial rise in deep-submicron noise through technology scaling severely effects the worth of domino circuits. By technology scaling, the supply voltage is topped down to drop the power consumption. In order to increase performance, the transistor threshold voltage has to be commensurately surmounted to keep a high drive current. On the other hand, the Vth (threshold voltage) mounting results in the considerable and increase of the sub-threshold leakage current.

Diode Footed Domino

The Diode Footed Domino (DFD) is appeared in Figure 2 demonstrates the alteration over footed domino rationale. The diode footer (transistor M1) decreases the sub-threshold leakage due to a phenomenon called the stacking effect. Because of the leakage of the evaluation transistors, there is certain voltage drop recognized across the diode footer (transistor M1) in the evaluation period. This voltage drop makes the gate-to-source voltage of the OFF evaluation transistors negative, causing an exponential reduction in the sub-threshold leakage. Furthermore, the voltage-drop through the diode rises the body effect of the evaluation transistors, which similarly supports in the sub-threshold leakage drop.

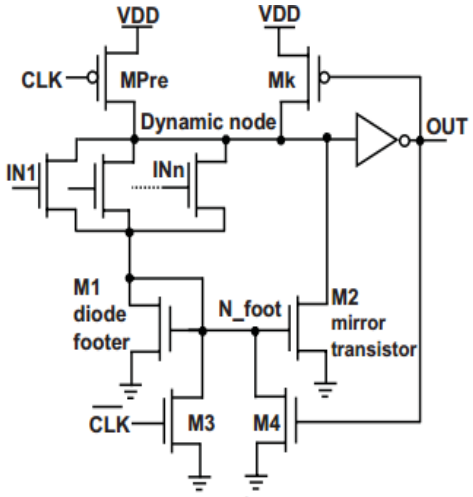

Figure 2: Diode footed domino logic

On the other hand, the diode footer increases the switching threshold voltage of the gate by the threshold of NMOS devices and hence, the new gate switching threshold voltage is about 2Vtn. The advanced gate switching voltage domino effect in a improved noise immunity, nevertheless, at the expenditure of performance dreadful conditions. The purpose for performance dreadful conditions is that the diode footer losses the evaluation current. To rise the performance, the mirror transistor (Figure 2) is used to mirror the evaluation current also drain it as of the precharge node (N_dyn). As a result, the total evaluation current is equivalent to the evaluation current over and done with the evaluation network and over the mirrored evaluation current.

Precharge phase

When CLK =0, the dynamic node is precharged to VDD by the PMOS transistor *Mp*. During that time the evaluation transistor *Me* is off, so that the pull down path is disabled. The evaluation FET eliminates any static power that would be consumed during the precharge period (i.e., static current would flow between the supplies if both the pull-down and the precharge device were turned on simultaneously). Output remains same as the input CLK because of inverted output.

Evaluation phase

For CLK =1 the precharge transistor *Mp* is off, and the evaluation transistor *Me* is turned on. The result is tentatively discharged built on the feedback (i/p) values and the pull-down topology. If the inputs are such that the PDN conducts, then a low resistance path exists between dynamic node and GND. If the pull-down network is turned off, the precharge value remain stored on the dynamic capacitance and output capacitance remain maintain with 0 value, which is a combination of junction capacitances, the wiring capacitances, and the input capacitances of the fan-out gates. For the duration of the evaluation process, the only possible path among the dynamic node and a source rail is to GND.

As a result, when dynamic node is discharged, it cannot be charged for a second time until the after precharge process. The inputs to the gate can thus make at most one transition during evaluation. Notice that the dynamic node can be in the high impedance state during the evaluation period if the pull-down network is turned off. This behavior is fundamentally different from the static counterpart that always has a low resistance path between the dynamic node and one of the power rails.

One of the advantage of domino logic over static logic can also be switches from a low to high direction, so no need of any input to drive pull-up PMOS transistors. The privation of PMOS transistor means that the active transistor size that loads down an earlier step of logic, for a specific current drive, favours domino in excess of static logic. This is grave then the key to great speed is make certain that a speed improvement can be grown without stuffing down.

Diode Footed Domino Comparator

The Diode Footed Domino (DFD) Comparator appeared in Figure 3 utilizes the idea of voltage detecting of the two terminals of the assessment organize PDN. During pre-charge phase, system clock is ‘0’, and all inputs become 0. Hence, at this time, dynamic node succeeds to pre charged over the M_{Pre} transistor, as an outcome the output of the comparator becomes zero. During evaluation phase, when the system clock is ‘1’, M_{Pre} transistor goes OFF turning the pull down network matures to active and conducts based upon the applied inputs logic levels.

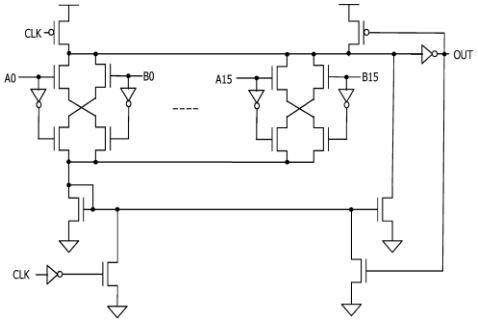

Figure 3: Diode footed domino comparator

If all the bits of input A and input B are equal and matching, there is no discharge path at dynamic node and GND. But, if applied level logic of input A and input B differ by a single bit position, a conducting rail is well-established between dynamic node and GND, resulting in discharging of the dynamic node. Hence, this leads the output node of comparator to go high, along with giving way for a worst case scenario for the delay.

The major problem in comparator design using diode footed domino logic is that; it fails to conduct correctly for smaller size of the keeper transistor Mk, as a result of high leakage current. As well, it scatters huge amount of energy on together: full match of input bits plus mismatch of input bits.

PROPOSED DOMINO CIRCUIT

The purpose of this circuit technique is to effectively enhance the reduction of the gate oxide leakage current and the sub-threshold leakage current simultaneously. Figure 4 shows the generalized structure of LECTOR technique.

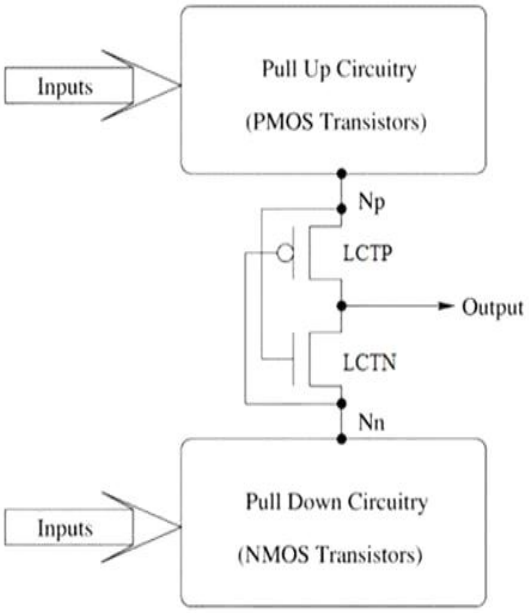

Figure 4: LECTOR (Leakage Controlled logic gates) technique

The perception in arrears this method for the decrease of leakage power is the use of in effect load up of transistors stuck between the paths from VDD to GND. The structure of lector based diode footed domino logic comparator shown in Figure 5.

In this method, dual leakage control transistors are LCTP (PMOS) and LCTN (NMOS). That introduced in the middle of the pull-up and pull-down network. These two gate transistors are controlled by the source terminal of each other here, transistor LCTP and LCTN's switching depends on the potential difference at node NP and NN, respectively. Hence, for any combination of applied input one of the lector transistors will operate near cut-off region, increasing the resistance between supply and ground rails leading to shrinking of the leakage current.

Non idle mode

During non-ideal mode (pre-charge mode), when the clock is low the dynamic node is debited to VDD through transistors, MPre and LCTP. The pre-charging of dynamic node is virtually autonomous of the input states.

If all the inputs act low ahead the clock is set to low then the node NN will hold at low voltage along with transistor LCTP bid the less resistance rail for charging dynamic nodule. If all the inputs applied act high, then the potential difference at node NN is insufficient for turning OFF LCTP completely i.e., LCTP is conducting adjacent its cut- off region. Therefore, resistance due to LCTP will act much lower than the completely OFF state resistance leading to high charging of the dynamic node. In this case, the leakage current be determined by, going on the applied inputs while; the comparator output is liberated of these feedbacks (i/p's).

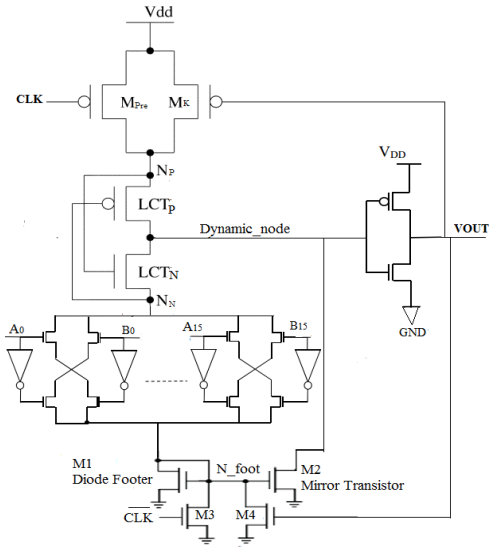

Figure 5: Lector based diode footed domino logic comparator

Idle mode

During ideal mode (evaluation mode), just as the clock is high, dynamic node gets discharged or charged depending upon the applied input vectors. If valid inputs are applied pull-down network transistors leakage current establishes some potential across diode footer, M1, which forms the OFF evaluation transistors gate-source-voltage negative. This results in exponential contraction in sub leakage current. Therefore, if sequences of inputs are equal and matching, the dynamic node will no longer be discharged by the pull-down network and the output concerning the comparator is low and it directs keeper transistor, MK, ON.

The potential at node NP will direct the transistor LCTN, ON, but potential at node NN will no longer allow the transistor LCTP to completely cut-off making it conduct adjacent cut-off-region leading to high resistance path amidst supply and ground shrinking the sub-threshold and gate leakage current. Here, if all the inputs are low, the LCTP will operate near cut-off-region and if all the applied inputs are high, the LCTN will conduct near cut-off-region. Hence, by employing LCTs, the resistance along the supply and GND is

enlarged which in turn reduces leakage current and concurrently increases the domino comparator circuits propagation delay. The proper sizing of the lector transistors, LCTP and LCTN, helps in controlling the propagation delay of the circuit.

SIMULATION RESULTS

Tanner EDA tool is a SPICE computer analysis programmed for analogue integrated circuits. Using these engine tools, spice program provides facility to design and simulate new ideas in analog integrated circuits before going to the time consuming and costly process of chip fabrication. Simulation setup of S-Edit window is shown in Figure 6.

Description of S-Edit is given below,

- Start S-Edit
- Start a New Design
- Create a new Cell
- Enter the symbol libraries:
- Setup the SPICE Models for the Generic_025 kit.

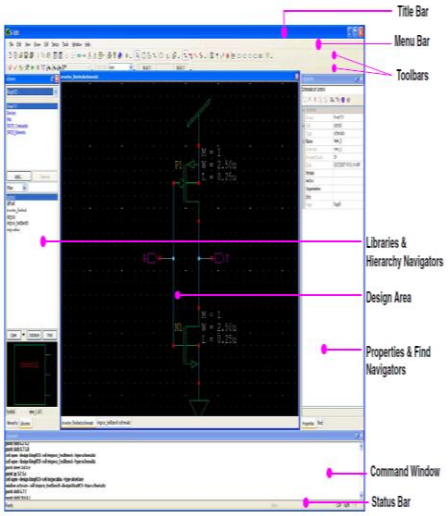

Figure 6: Simulation setup of S-Edit window

Schematic view of lector based diode footed domino comparator is shown in Figure 7. S-Edit is a schematic entry tool that is conditioned manuscript circuits that can be ambitious frontward into a layout of an integrated circuit (IC). It as well be responsible for the capability to achieve SPICE virtual reality of the circuits via a simulation engine that is called T-SPICE. T-SPICE can be outfit and entreated from within S-edit. SPICE models for the Generic_025 kit of figure is shown in Figure 8.

Tanner T-Spice virtual reality delivers fast and accurate simulation for analog and mixed-signal system (AMS) integrated circuit designs. T-Spice not only act out circuits rapidly with a high degree of accuracy, nevertheless as well is well-suited with industry most important standards and mixes easily with the Tanner S-Edit schematic capture tool and Tanner W-Edit.

T-Spice consist of better accuracy with forward-looking modelling, multi-threading livelihood, device state scheming, real-time waveform broadcasting and exploration, and a thorough knowledge wizard for simple SPICE syntax conception.

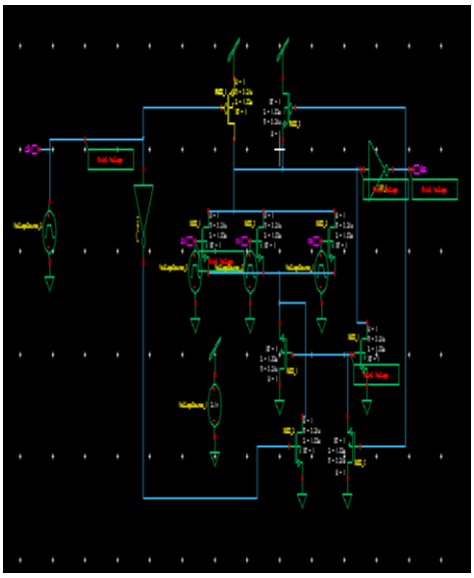

Figure 7: Schematic view of diode footed domino logic circuit

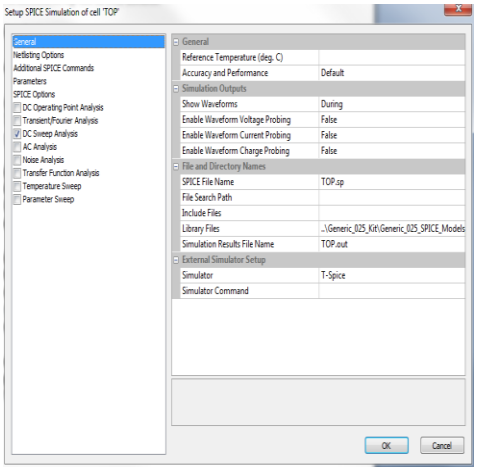

Figure 8: SPICE models for the Generic_025 kit

T-Spice implements fast and perfect simulation of analog and mixed analog/digital circuits. The simulator contains the most recent and best device models offered, as well as combined line models and livelihood for user defined device models via tables or C functions. Net-list View of T-SPICE window is shown in Figure 9.

T-Spice procedures an extended description of the SPICE input language that is companionable with all industry standard SPICE simulation programs. Totally SPICE's device models are integrated, as well as resistors(R), capacitors(C), inductors(L), mutual inductors, single and coupled transmission lines, current sources(I), voltage sources(V), controlled sources, and a full complement of the latest advanced semiconductor device simulations from Berkeley and Philips Labs. Figure 10 shows the programmers editor window.

In W-Edit charts can automatically configure for the type of data being presented. Chart views can be panned back and forth and zoomed in and out, specifying the exact X-Y coordinate ranges. W-Edit shows T-Spice simulation yield waveforms as they are presence of created during simulation. Figure 11 shows the simulated result of lector based diode footed domino comparator.

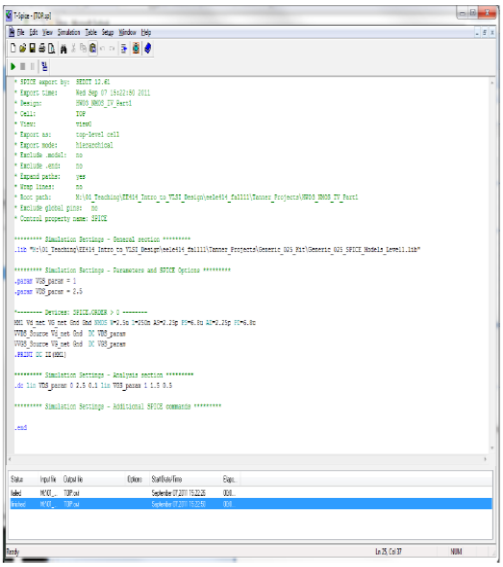

Figure 9: Net-list view of T-SPICE

Imagining the intricate numerical data resultant from VLSI circuit simulation is dangerous to test, understand, and improve those circuits. W-Edit is a waveform observer that offers simplicity of use, power, and speed in a supple environment intended for graphical data exhibition.

It provides the facility of,

- Design simulation
- Device statement
- Simulation commands
- User designed external models
- Small signal and noise models

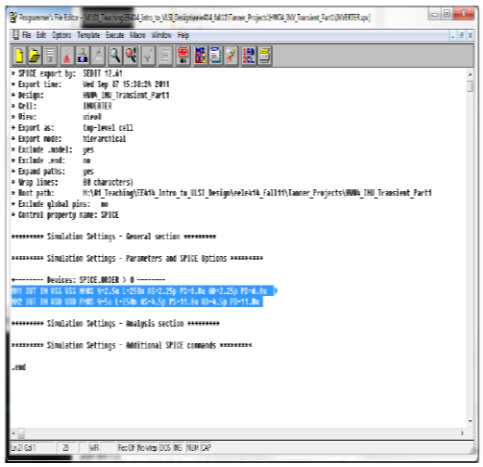

Figure 10: Programmer's editor window

The benefits of W-Edit includes

- Constricted integration with T-Spice, Tanner EDA's circuit-level simulator. W-Edit can graphic representation data created by T-Spice straight, without alteration of the output data files. W-Edit graphic representation data enthusiastically as it is created during the simulation.
- Graphic representation are robotically constructed for the type of data actuality offered.
- An information set is preserved by W-Edit as a unit called a trace. Several traces commencing different output files can be observed instantaneously, in solitary or manifold

windows. You can copy and move traces among graphic representation and frames. You can achieve trace arithmetic or spectral analysis on in effect traces to generate new ones.

- You can sauce pan back and forth and zoom in and out of chart views, as well as requiring the particular *x-y* coordinate range W-Edit displays. You can portion positions and distances flanked by points simply and exactly with the mouse.

You can make especially material goods of axes, traces, grids, charts, text, and colors. W-Edit is a waveform observer that provides ease of use, power speed in a stretchy environment intended for graphical chart.

L-edit is an IC physical design tool from Tanner EDA. This apparatus tolerates you to draw the layout of an integrated circuit, look at cross-sections, perform design rule check (DRC), and create a Net list of your layout so that you can achieve layout versus schematic (LVS) using a altered tool.

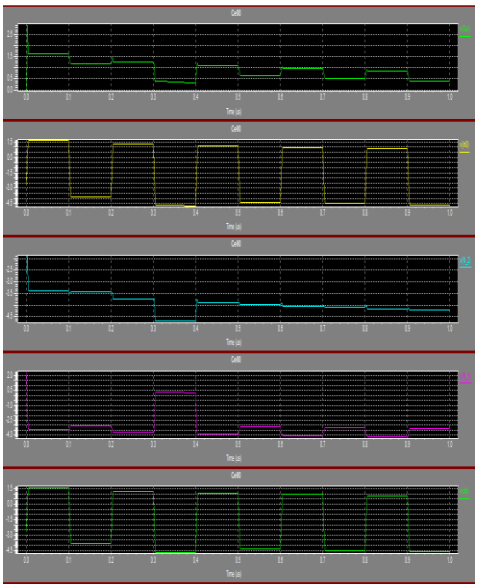

Figure 11: Simulated waveform of lector based diode footed domino comparator

Description of L-Edit is given below,

- Log onto a computer and launch L-edit
- Create a new layout design
- Verify the technology rule options & setup grid Save design

We continuously want to certify that the layout we have formed is what we proposed in the schematic. LVS will compare the Net list exported from S-edit and the Net list exported from L-edit. Here, not using L-Edit for implementing process. Only use S-Edit, T-Edit and W-Edit.

W-Edit is vigorously connected to T-Spice and S-Edit by a run-time apprise feature that shows simulation results for instance they are animation created and permits waveform cross-probing unswervingly in the schematic managing editor for earlier design cycles.

CONCLUSION

The power, delay and power delay product of the various domino logic has been analyzed and in diode footed domino the power delay product is 75% efficient compared to other conventional domino logic this is listed out in the Table I.

Table I: PDP result analysis of different domino logic

LOGIC	DELAY	POWER	PDP
Dynamic	4.50E-6	879E-9	3.959E-12
Domino	3.075E-6	2.988E-6	9.173E-12
High speed domino	4.754E-6	1.30E-6	6.209E-12
Diode footless domino	3.4E-11	1.26E-04	3.834E-15
Diode footed domino	5.8E-11	2.62E-5	8.0E-14

The Performance analysis of designed 16- bit footed domino logic comparator and 16- bit lector based diode footed domino logic comparator is summed up in the form of Table II. Figure 12 shows that power, delay and PDP analysis of different domino logic.

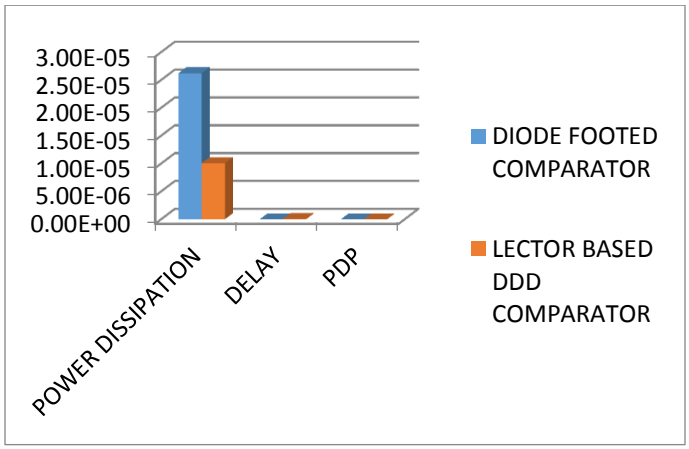

Figure 12: Power, delay and PDP analysis of different domino logic.

Table II: Comparison of different dominos

CONSTRAINTS	EXISTING METHOD	PROPOSED METHOD
Power dissipation	26.23uW	10.06uW
Delay	30.58ps	52.56ps
PDP	0.821fWs	0.528fWs

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