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### Optimization of speed and power by using 14T sram single bit cell

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#### ABSTRACT

For radiation hardening, using 14T SRAM bit cell, which circuit and layout level optimization design in a 65-nm CMOS technology increased pliability to single-event upset (SEU) as well as single-event-multiple-node upsets (SEMNUs) due to the charge sharing among OFF-transistors. In this proposed design of RSP-14T by 8-bit SRAM cell, which performance better than existing design of RSP-14T per bit. In this design CMOS transistors which is used to store the data. In the radiation environment, when the heavy ion incident occur on the semiconductor material, the particles will be ionized. These excess charges will be collected by the sensitive nodes of the device. As a result, a voltage perturbation will appear at those nodes. For SRAM bit cell, when the amplitude of the voltage perturbation is strong enough and exceeds the logic threshold level of the inverter, the data stored might be turned over. By using this concept of 14T SRAM design will give the better result of power, area and delay than the existing system. Finally, the proposed design is implemented in the TANNER EDA at 45nm CMOS Technology with 0.9V input voltage and proved the comparison in terms of area power and delay.

**Keywords:** High speed, Low power, Radiation-hardened SRAM, Single-event-multiple-node upsets (SEMNUs), Single-event upset (SEU).

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#### INTRODUCTION

Single-event upset (SEU) is a soft-error and nondestructive form of single-event effects (SEEs) [1]. In the radiation environment, when the heavy ion is incident on the semiconductor material, the particles will be ionized. These excess charges will be collected by the sensitive nodes of the device. As a result, a voltage perturbation will appear at those nodes. For SRAM bitcell, when the amplitude of the voltage perturbation is strong enough and exceeds the logic threshold level of the inverter, the data stored might be turned over, as shown in Fig. 1; that is, an SEU is caused. With the continuous scaling of CMOS technology, the minimum spacing between the transistors is decreased. As a result, multiple transistors are susceptible to the charge deposited from a single particle strike compared to older processes where only one transistor was affected [2]. The charge

sharing results in single-event-multiple-node upsets (SEMNUs), which is becoming the main effect of energetic particle strikes in emerging nanometer CMOS technology [3], [4]. In addition, supply voltage reduction further increases the susceptibility of circuits to radiation. Thus, the development of radiation-hardened technologies in digital circuits is extremely urgent [5]. Due to the larger sensitive volume per bit and lower node capacitance than the dynamic counterpart, SRAM is more prone to soft errors. Therefore, the soft error rate (SER) [6] in SRAM is increased with the technology scaled in the nanometer regime. In order to reduce the SER, numerous alternatives have been proposed to the standard 6T SRAM cell [7]–[15]. The main reinforcement method is through constructing special topology of transistor connections inside cells to achieve circuit-level protection. The soft error robust Quatro-10T SRAM cell, offering differential read operation

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with large noise margin was proposed in [7]. However, it can only recover from “1” to “0”; thus, it cannot immune SEU completely. Due to the feedback of the dual node, the dual interlocked storage cell (DICE) [8] can fully immune against single-event transient (SET) occurring on any of its single nodes. However, the very minimum ability of SEMNUs immunity and radiation hardness performance of it has yet to be improved. In [4], based on Schmitt trigger, the Schmitt trigger based (STB)-13T memory cell with fully SEU immune was proposed. However, the limited promotion of SEMNUs immunity ability of it is achieved at the expense of writing speed, power consumption, and layout area compared with DICE. Based on the STB13T, two novel hardened memory cells with more reliability, radiation hardened design (RHD)-11T and RHD-13T, were proposed in [9]. Unfortunately, the writing speed, as well as write margin, of them is deteriorated. In [10], for low power and highly reliable radiation-hardened application, the RH memory (RHM)-12T was proposed; however, the authors used nMOS as pull-up devices causing worse read noise margins. Recently, the RHD-12T memory cell with favorable radiation hardness performance, as shown in Fig. 2(a), was proposed in [12]. Besides the toleration for an SEU on any of its internal single nodes, it can also provide the SEMNUs immunity to some extent. Unfortunately, the slow write speed as well as large power consumption limits the application of it. In addition to the reinforcement at the circuit level, specific layout techniques as an alternative method for improving the radiation tolerance have also been proposed [13], [14]. As presented in [13], a new layout technique named layout design through error-aware transistor positioning (LEAP) was applied to DICE, resulting in a new sequential element, LEAP-DICE. The TCAD simulations show that it is effective for increasing the linear energy transfer (LET) upset threshold. In order to investigate the charge sharing, a Monte Carlo simulation platform named tool suite for radiation reliability assessment (TIARA) was given in [14]. By analysis of the TIARA simulations results, the layout optimization of the most vulnerable transistor pairs will be targeted.

## LITERATURE SURVEY

P. E. Dodd and L. W. Massengill, “Basic mechanisms and modeling of single-event upset in digital microelectronics,” - Physical mechanisms responsible for nondestructive single-event effects in digital microelectronics are reviewed, concentrating on silicon MOS devices and integrated circuits. A brief historical overview of single-event effects in space and terrestrial systems is given, and upset mechanisms in dynamic random access memories, static random access memories, and combinational logic are detailed. Techniques for mitigating single-event upset are described, as well as methods for predicting device and circuit single-event response using computer simulations. The impact of technology trends on single-event susceptibility and future areas of concern are explored.

J. D. Black, P. E. Dodd, and K. M. Warren, “Physics of multiple-node charge collection and impacts on single-event characterization and soft error rate prediction,” - Physical mechanisms of single-event effects that result in multiple-node charge collection or charge sharing are reviewed and summarized. A historical overview of observed circuit responses is given that concentrates mainly on memory circuits. Memory devices with single-node upset mechanisms are shown to exhibit multiple cell upsets, and spatially redundant logic latches are shown to upset when charge is collected on multiple circuit nodes in the latch. Impacts on characterizing these effects in models and ground-based testing are presented. The impact of multiple-node charge collection on soft error rate prediction is also presented and shows that full circuit prediction is not yet well understood. Finally, gaps in research and potential future impacts are identified.

M. Fazeli, S. N. Ahmadian, S. G. Miremadi, H. Asadi, and M. B. Tahoori, “Soft error rate estimation of digital circuits in the presence of multiple event transients (METs),” - In this paper, we present a very fast and accurate technique to estimate the soft error rate of digital circuits in the presence of Multiple Event Transients (METs). In the proposed technique, called Multiple Event Probability Propagation (MEPP), a four-value logic and probability set are used to accurately

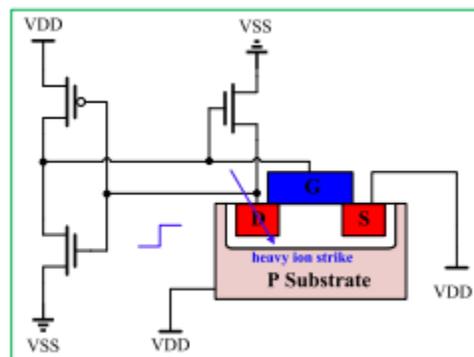
propagate the effects of multiple erroneous values (transients) due to METs to the outputs and obtain soft error rate. MEPP considers a unified treatment of all three masking mechanisms i.e., logical, electrical, and timing, while propagating the transient glitches. Experimental results through comparisons with statistical fault injection confirm accuracy (only 2.5% difference) and speed-up (10,000X faster) of MEPP.

S. Lin, Y.-B. Kim, and F. Lombardi, "Analysis and design of nanoscale CMOS storage elements for single-event hardening with multiple-node upset,"- The occurrence of a single event with a multiple-node upset is likely to increase significantly in nanoscale CMOS due to reduced device size and power supply voltage scaling. This paper presents a comprehensive treatment (model, analysis, and design) for hardening storage elements (memories and latches) against a soft error resulting in a multiple-node upset at 32-nm feature size in CMOS. A novel 13T memory cell configuration is proposed, analyzed, and simulated to show a better tolerance to the likely multiple-node upset. The proposed hardened memory cell utilizes a Schmitt trigger (ST) design. As evidenced in past technical literature and used in this work, simulation of all node pairs by current sources results in an assessment similar to 3-D device tools; the simulation results show that the proposed 13T improves substantially over DICE in the likely and realistic scenarios of very diffused or limited charge sharing/collection. Moreover, the

13T cell achieves a 33% reduction in write delay and only a 5% (9%) increase in power consumption (layout area) compared to the DICE cell (consisting of 12 transistors). The analysis is also extended to hardened latches; it is shown that the latch with the highest critical charge has also the best tolerance to a multiple-node upset. Among the hardened latches, the ST designs have the best tolerance, and in particular, the transmission gate configuration is shown to be the most effective. Simulation results are provided using the predictive technology file for 32-nm feature size in CMOS. Monte Carlo simulation confirms the excellent multiple-node upset tolerance of the proposed hardened storage elements in the presence of process, voltage, and temperature variations in their designs.

### Existing System

Single-event upset (SEU) is a soft-error and nondestructive form of single-event effects (SEEs). In the radiation environment, when the heavy ion is incident on the semiconductor material, the particles will be ionized. These excess charges will be collected by the sensitive nodes of the device. As a result, a voltage perturbation will appear at those nodes. For SRAM bit cell, when the amplitude of the voltage perturbation is strong enough and exceeds the logic threshold level of the inverter, the data stored might be turned over, as shown in Fig. 1; that is, an SEU is caused.



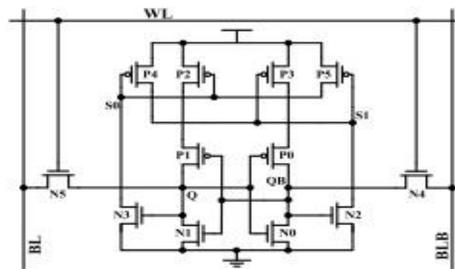
**Figure 1: SEU induced by an ion strike in an SRAM memory**

With the continuous scaling of CMOS technology, the minimum spacing between the transistors is decreased. As a result, multiple

transistors are susceptible to the charge deposited from a single particle strike compared to older processes where only one transistor was affected.

The charge sharing results in single-event-multiple-node upsets (SEMNUs), which is becoming the main effect of energetic particle strikes in emerging nanometer CMOS technology. In addition, supply voltage reduction further increases the susceptibility of circuits to radiation. Thus, the development of radiation-hardened technologies in digital circuits is extremely urgent. Due to the larger sensitive volume per bit and lower node capacitance than the dynamic counterpart, SRAM is more prone to soft errors. Therefore, the soft error rate (SER) in SRAM is increased with the technology scaled in the nanometer regime. In order to reduce the SER, numerous alternatives have been proposed to the standard 6T SRAM cell. The main reinforcement method is through constructing special topology of transistor connections inside cells to achieve circuit-level protection. The soft error robust Quatro-10T SRAM cell, offering differential read operation with large noise margin was proposed. However, it can only recover from “1” to “0”; thus, it cannot immune SEU completely. Due to the

feedback of the dual node, the dual interlocked storage cell (DICE) can fully immune against single-event transient (SET) occurring on any of its single nodes. However, the very minimum ability of SEMNUs immunity and radiation hardness performance of it has yet to be improved. Based on Schmitt trigger, the Schmitt trigger based (STB)-13T memory cell with fully SEU immune was proposed. However, the limited promotion of SEMNUs immune ability of it is achieved at the expense of writing speed, power consumption, and layout area compared with DICE. Based on the STB13T, two novel hardened memory cells with more reliability, radiation hardened design (RHD)-11T and RHD-13T, were proposed. Unfortunately, the writing speed, as well as write margin, of them is deteriorated. For low power and highly reliable radiation-hardened application, the RH memory (RHM)-12T was proposed; however, the authors used nMOS as pull-up devices causing worse read noise margins. Recently, the RHD-12T memory cell with favorable radiation hardness performance, as shown in Fig. 2.



**Figure 2: RHD-12T bit cell.**

Besides the toleration for an SEU on any of its internal single nodes, it can also provide the SEMNUs immune to some extent. Unfortunately, the slow write speed as well as large power consumption limits the application of it. In addition to the reinforcement at the circuit level, specific layout techniques as an alternative method for improving the radiation tolerance have also been proposed. As presented in, a new layout technique named layout design through error-aware transistor positioning (LEAP) was applied to DICE, resulting in a new sequential element, LEAP-DICE. The TCAD simulations show that it

is effective for increasing the linear energy transfer (LET) upset threshold. In order to investigate the charge sharing, a Monte Carlo simulation platform named tool suite for radiation reliability assessment (TIARA) was given. By analysis of the TIARA simulations results, the layout optimization of the most vulnerable transistor pairs will be targeted.

In this paper, the radiation-hardened with speed and power optimized (RSP)-14T bit cell is proposed. Compared with RHD-12T, its radiation hardness has been improved by the reinforcement of redundant nodes with two extra pMOS

transistors. Furthermore, due to the supply of the branch where the redundant nodes located are controlled by the extra PMOSs, during the write operation, the feedback mechanism will be interrupted easily. Thus, the write speed and power consumption have been improved effectively. Generally, SPICE simulations by using the double-exponential current source model are applied for evaluating the radiation tolerance of the circuit, which is time saving. However, the model relies on calibration parameters that are not physical. The charge sharing between transistors will be neglected; it may overestimate the SEU immune ability of other SRAM cells. Thus, in order to consider the charge sharing between transistors as well as reducing the CPU burden, TCAD mixed-mode simulation as a good qualitative approach to evaluate SEU immune is adopted in this paper. Combined with the layout-level design, the simulation results show that the proposed circuit has better SEU immunity.

### Disadvantages

- During the write operation, the feedback mechanism will be interrupted easily.
- The charge sharing between transistors will be neglected.

### PROPOSED SYSTEM

For radiation hardening, using 14T SRAM bit cell, which circuit and layout level optimization

design in a 65-nm CMOS technology increased pliability to single-event upset (SEU) as well as single-event-multiple-node upsets (SEMNU) due to the charge sharing among OFF-transistors. In this proposed design of RSP-14T by 8-bit SRAM cell, which performance better than existing design of RSP-14T per bit. In this design CMOS transistors which is used to store the data. In the radiation environment, when the heavy ion incident occur on the semiconductor material, the particles will be ionized. These excess charges will be collected by the sensitive nodes of the device. As a result, a voltage perturbation will appear at those nodes. For SRAM bit cell, when the amplitude of the voltage perturbation is strong enough and exceeds the logic threshold level of the inverter, the data stored might be turned over. By using this concept of 14T SRAM design will give the better result of power, area and delay than the existing system.

### Read and Write Operation

The schematic of the proposed RSP-14T is shown in Fig.3. Here, the transistors N4 and N5, controlled by a word line (WL), are access transistors, which control the connection between the bit lines (BL and BLB) and the storage nodes (Q and QB). The nodes S1 and S0 are redundant nodes of Q and QB. If the stored bit is "1," the logic values at nodes Q, QB, S1, and S0 are "1," "0," "1," and "0," respectively.

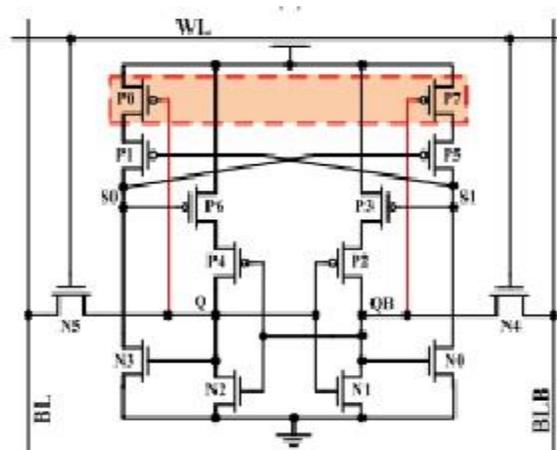


Figure 3: Proposed RSP-14T bitcell.

The functional analysis of the proposed RSP-14T is sequentially presented: 1) write; 2) read; and 3) hold operation. In write operation, we assume that  $Q = "1"$  and  $QB = "0"$  and the bit lines BL and BLB are set to "0" and "1," respectively. When the WL is activated, the value stored in Q and QB will be changed to "0" and "1," respectively. After that, once WL is discharged to "0," the new state of the memory cell is stored. For a read operation, the BL and BLB are precharged to "1." When the selected WL is enabled, the transistors N4 and N5 are turned on, BLB will be discharged through transistors N4 and N1. As a result, the differential voltage of the BLs will be generated and amplified by the sense amplifier. During the hold operation, WL is deactivated and the storage nodes are isolated from the BLs; thus, they maintain the initial state. In this paper, the transistors P0 and P7 are used to control the connection or cutoff between the power supply and transistors P1/P5, which is beneficial to improve the write speed and power consumption compared with RHD-12T.

### Error Tolerance Analysis

Regardless of the charge sharing between the transistors in the actual layout, the analyses of SEU recovery behavior at circuit level are given. Assuming that  $Q = "1,"$   $QB = "0,"$   $S1 = "1,"$  and  $S0 = "0,"$  respectively, the analyses of the nodes (Q, QB, S1, and S0) are demonstrated as follows.

**Case 1 (Positive Transient Pulse at Node S0):** When the drain of P1 is hit by a particle, it will collect positive charge and increase the voltage at node S0 (i.e., S0 will be changed from "0" to "1"). As a result, P6 and P5 will be turned off. However, it cannot further affect the OFF/ON-states of other transistors, and the storage status of Q and S1 nodes will remain unchanged. Therefore, the transient fault at S0 cannot propagate inside the cell. Finally, the nodal logic level will be recovered after the radiation events.

**Case 2 (Positive Transient Pulse at Node QB):** When the drain of P2 is hit by a particle, it will collect positive charge and increase the voltage at node QB (i.e., QB will be changed from "0" to "1"). As a result, N2 and N0 will be turned on. Correspondingly, Q and S1 will be changed from "1" to "0," P0 and P1 will be turned on, and N3

will be turned off, and then S0 will be changed from "0" to "1." Finally, the storage state of the cell will be turned over. (It has been made difficult to change in the layout-level design as presented in Section III.) Due to the transistors being stacked and topology optimized, the parasitic bipolar amplification effect of P2 (the source of P3 is connected with VDD, whereas the source of P2 with weak connection "1") is mitigated. As a result, the quantity of charge collected by the drain of P2 is reduced, which improves the SEU tolerance of node QB.

**Case 3 (Negative Transient Pulse at Node S1):** When the drain of N0 is hit by a particle, it will collect negative charge and S1 will be discharged from "1" to "0," and P3 and P1 will be turned on. However, due to the blocking effect of transistors P2 and P0, the fault at S1 cannot further propagate in the cell. Therefore, QB and S0 will remain in their original status. Due to the low status at QB and S0, P7 and P5 are always at open state. Hence, the current provided by P7 and P5 will charge S1 continuously. This positive feedback will accelerate the recovery process of S1. Finally, the nodal storage status will be recovered after the radiation events.

**Case 4 (Negative Transient Pulse at Node Q):** When the drain of N2 is hit by a particle, negative charge will be collected and Q will be discharged from "1" to "0," and then N1 and N3 will be turned off. This is very similar to case 1, thus, the storage status of Q will finally recover after the radiation events. For time efficiency, in order to prove that the above-mentioned analyses are correct and locate the most vulnerable node of the proposed RSP-14T, the transient injections at S0, QB, S1, and Q nodes are simulated, by the double-exponential current source. On this basis, further analysis of SEU is given by TCAD in Section III. Here, the double-exponential current is expressed as

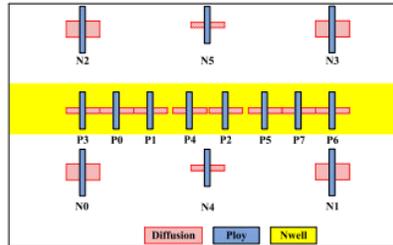
$$I(t) = I_0(e^{-t/\tau\alpha} - e^{-t/\tau\beta}) \dots\dots\dots(1)$$

$$I_0 = Q/(\tau\alpha - \tau\beta) \dots\dots\dots(2)$$

Where  $I_0$  is the peak of current source, Q is the amount of deposited charge,  $\tau\alpha$  is the collection time constant of the junction, and  $\tau\beta$  is the time constant for initially establishing the ion track. In this paper,  $I_0$  is set as  $\sim 174 \mu A$ , while  $\tau\alpha$  and  $\tau\beta$  are set as 200 and 50 ps, respectively.

From the above-mentioned analyses and simulation results, it is observed that QB (or Q depending on whether the node stores “0”) is the most vulnerable node. Thus, it is essential to make it stronger through the layout-level design. As illustrated in

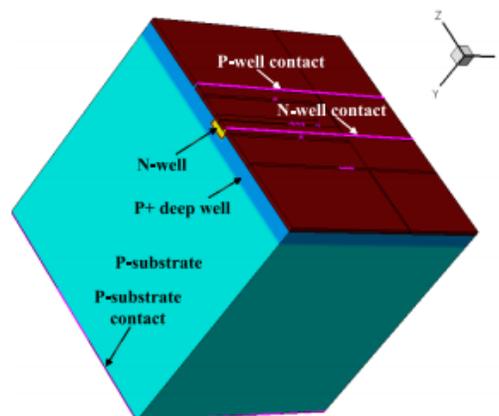
Fig. 3, the drains of the OFF-transistors are the sensitive areas. When the drain of P2 (OFF-state) is struck, many holes will be injected into the n-well



**Figure 4: Transistors placement of the proposed RSP-14T.**

From the VDD due to the bipolar effect. Consequently, the number of holes collected by the drain will be increased. Therefore, mitigating the bipolar effect in the pMOS connecting the storage node is a prior selection for enhancing the SRAM SEU immune. The source isolation technique, which has been proven highly effective in mitigating p-hit SET and presented, is adopted for the proposed structure to complete the strengthening of the node. On this basis, in order to further mitigate the upset from “0” to “1” (occurring on node QB), the special design of stacking pMOS transistors with layout-level optimization is also adopted simultaneously. As

discussed in case 2, when the drain of P2 is struck, N0 and N2 will be affected, which fosters the upset of the SRAM cell. Therefore, in order to avoid charge sharing, the OFF-transistor N0 together with N2 should be distant from the other OFF-pMOS transistors. Similarly, P2 and P3 should be also distant from each other to prevent them from turning on at the same time. For layout-level optimization, the transistors placement of the proposed RSP-14T is shown in Fig. 3. With the above-mentioned circuit- and layout-level optimization, QB of the proposed RSP-14T can be as strong as possible. This deduction will be proven through the TCAD mixed-mode simulation.



**Figure 5: TCAD model and the top view of the proposed RSP-14T**

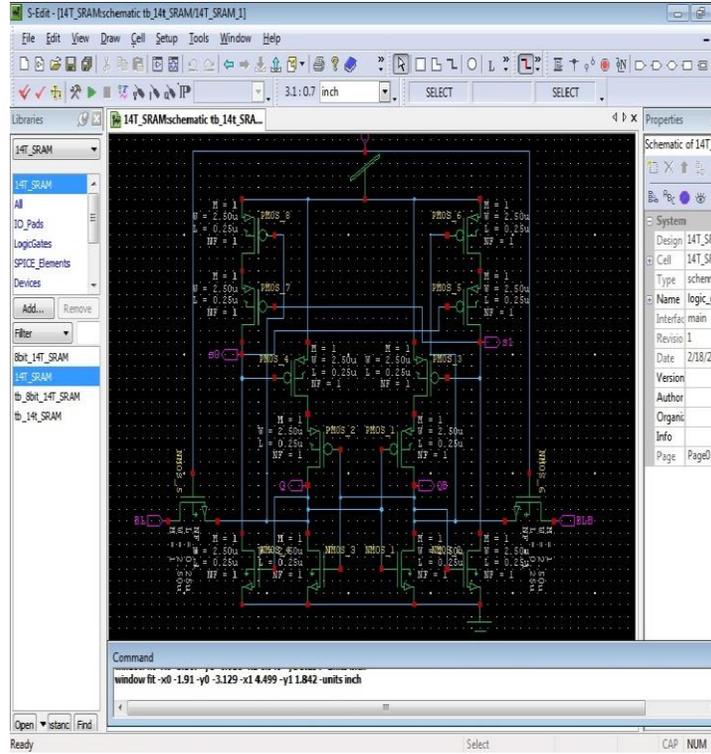
### Advantages

- During the write operation, the feedback mechanism will not be interrupted easily.
- Requires low area.

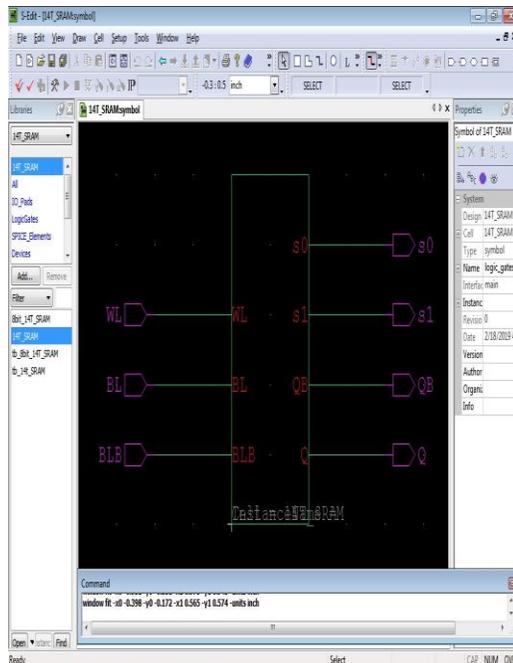
## RESULT AND DISCUSSION

### S edit output

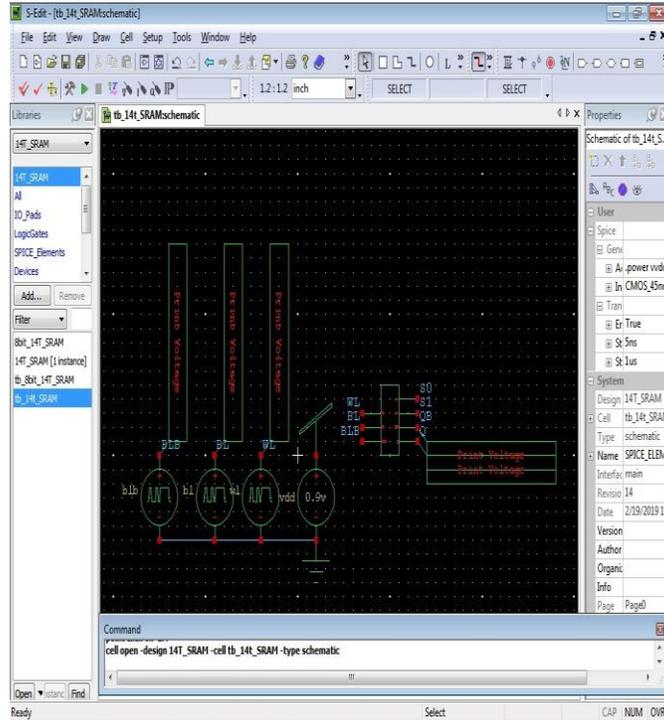
Existing RSP-14T SRAM 1 bit



Block Diagram of Existing RSP-14T SRAM 1 bit

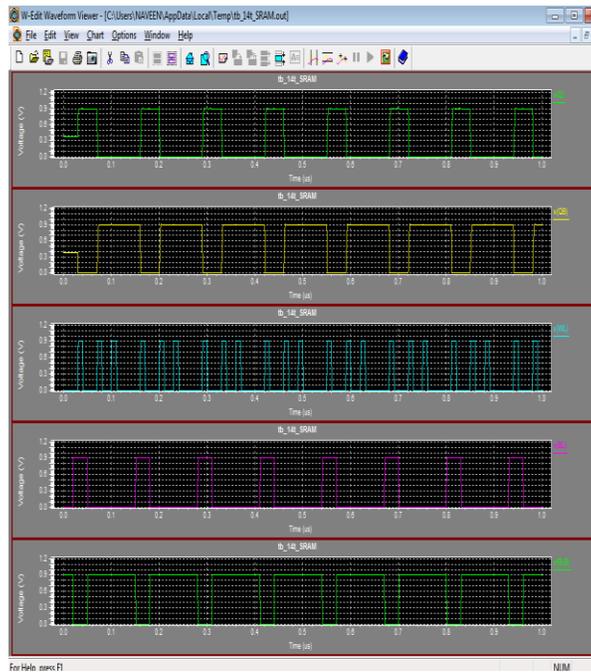


## Test bench of Existing RSP-14T SRAM 1 bit

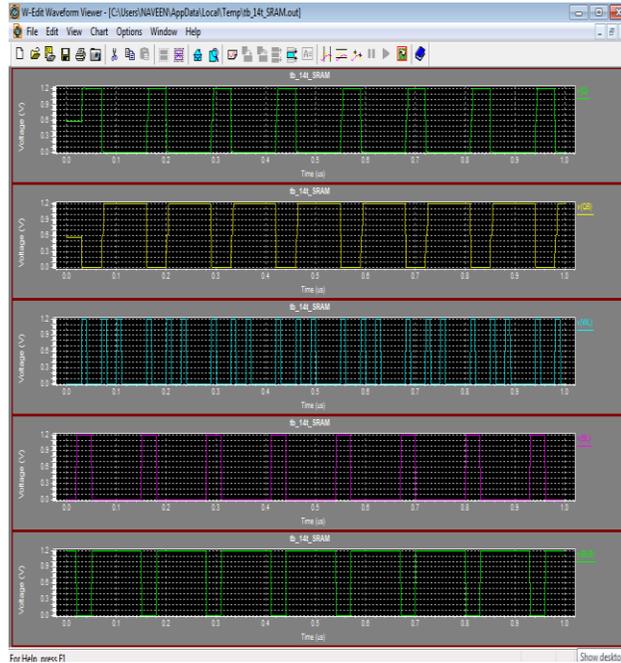


## W-edit output

## Existing RSP-14T SRAM 1 bit (45)

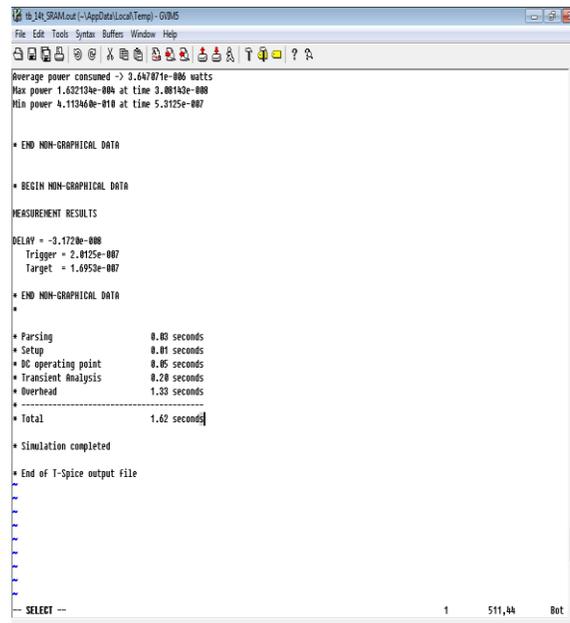


## Existing RSP-14T SRAM 1 bit (65)



## POWER RESULT

## Existing RSP-14T SRAM 1 bit (65 nm)



## Existing RSP-14T SRAM 1 bit (45 nm)

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t0_14t_SRAM.out (-AppData\Local\Temp) - GWIN
File Edit Tools Syntax Buffers Window Help
Min power 4.414891e-010 at time 9.2125e-007

* END NON-GRAPHICAL DATA
* BEGIN NON-GRAPHICAL DATA
MEASUREMENT RESULTS
DELAY = -9.9984e-010
Trigger = 2.0100e-007
Target = 2.0000e-007
* END NON-GRAPHICAL DATA
*
* Parsing          0.02 seconds
* Setup            0.00 seconds
* DC operating point 0.01 seconds
* Transient Analysis 0.20 seconds
* Overhead         1.33 seconds
*-----
* Total            1.56 seconds
* Simulation completed
* End of T-Spice output file
480,26 Bot

```

## CONCLUSION

In this paper, the radiation-hardened 14T SRAM 8 bit cell with speed and power optimized (RSP-14T) based on the source isolation technique is presented. Through the circuit- and layout-level optimization, trigger delay is adequate, which is larger than that reported for RSP-14T. Meanwhile, compared with RSP-14T 1 bit cell, its write speed

is significantly improved, but power consumption is large. It requires less area to implement and the proposed RSP-14T 8 bit cell is more suitable for the space application. In Future To design a Radiation-Hardened 14-Transistor SRAM Bit Cell to 8-Bit with 45nm and 65nm and proved the comparisons.

## REFERENCE

- [1]. P. E. Dodd and L. W. Massengill, "Basic mechanisms and modeling of single-event upset in digital microelectronics," *IEEE Trans. Nucl. Sci.*, 50(3), 583–602, 2003.
- [2]. J. D. Black, P. E. Dodd, and K. M. Warren, "Physics of multiple-node charge collection and impacts on single-event characterization and soft error rate prediction," *IEEE Trans. Nucl. Sci.*, 60(3), 2013, 1836–1851.
- [3]. M. Fazeli, S. N. Ahmadian, S. G. Miremadi, H. Asadi, and M. B. Tahoori, "Soft error rate estimation of digital circuits in the presence of multiple event transients (METs)," in *Proc. IEEE Int. Conf. Design, Automat. Test Eur.*, 2011, 70–75.
- [4]. S. Lin, Y.-B. Kim, and F. Lombardi, "Analysis and design of nanoscale CMOS storage elements for single-event hardening with multiple-node upset," *IEEE Trans. Device Mater. Rel.*, 12(1), 2012, 68–77.
- [5]. E. Ibe, H. Taniguchi, Y. Yahagi, K. Shimbo, and T. Toba, "Impact of scaling on neutron-induced soft error in SRAMs from a 250 nm to a 22 nm design rule," *IEEE Trans. Electron Devices*, 57, 2010, 1527–1538.
- [6]. R. C. Baumann, "Soft errors in advanced semiconductor devices-part I: The three radiation sources," *IEEE Trans. Device Mater. Rel.*, 1(1), 2001, 17–22.

- [7]. S. M. Jahinuzzaman, D. J. Rennie, and M. Sachdev, "A soft error tolerant 10T SRAM bit-cell with differential read capability," *IEEE Trans. Nucl. Sci.*, 56(6), 2009, 3768–3773.
- [8]. T. Calin, M. Nicolaidis, and R. Velazco, "Upset hardened memory design for submicron CMOS technology," *IEEE Trans. Nucl. Sci.*, 46(6), 1996, 2874–2878.
- [9]. R. Rajaei, B. Asgari, M. Tabandeh, and M. Fazeli, "Design of robust SRAM cells against single-event multiple effects for nanometer technologies," *IEEE Trans. Device Mater. Rel.*, 15(3), 2015, 429–436.
- [10]. J. Guo, L. Xiao, and Z. Mao, "Novel low-power and highly reliable radiation hardened memory cell for 65 nm CMOS technology," *IEEE Trans. Circuits Syst. I, Reg. Papers*, 61(7), 2014, 1994–2001.
- [11]. H. B. Wang et al., "An area efficient SEU-tolerant latch design," *IEEE Trans. Nucl. Sci.*, 61, 2014, 3660–3666.
- [12]. C. Qi, L. Xiao, T. Wang, J. Li, and L. Li, "A highly reliable memory cell design combined with layout-level approach to tolerant single-event upsets," *IEEE Trans. Device Mater. Rel.*, 16(3), 2016, 388–395.
- [13]. L. H.-H. Kelin et al., "LEAP: Layout design through error-aware transistor positioning for soft-error resilient sequential cell design," in *Proc. IEEE Int. Rel. Phys. Symp.*, 2010, 203–212.
- [14]. S. Uznanski, G. Gasiot, P. Roche, J.-L. Autran, and V. Ferlet-Cavrois, "Monte-Carlo based charge sharing investigations on a bulk 65 nm RHBD flip-flop," *IEEE Trans. Nucl. Sci.*, 57(6), 2010, 3267–3272.
- [15]. H.-B. Wang et al., "An area efficient stacked latch design tolerant to SEU in 28 nm FDSOI technology," *IEEE Trans. Nucl. Sci.*, 63(6), 2016, 3003–3009.
- [16]. D. A. Black, W. H. Robinson, I. Z. Wilcox, D. B. Limbrick, and J. D. Black, "Modeling of single event transients with dual doubleexponential current sources: Implications for logic cell characterization," *IEEE Trans. Nucl. Sci.*, 62(4), 2015, 1540–1549.
- [17]. J. Chen, S. Chen, B. Liang, B. Liu, and F. Liu, "Radiation hardened by design techniques to reduce single event transient pulse width based on the physical mechanism," *Microelectron. Rel.*, 52, 2012, 1227–1232.
- [18]. J. Chen, S. Chen, B. Liang, and B. Liu, "Simulation study of the layout technique for P-hit single-event transient mitigation via the source isolation," *IEEE Trans. Device Mater. Rel.*, 12(2), 2012, 501–509.
- [19]. C. Peng et al., "A radiation harden enhanced Quatro (RHEQ) SRAM cell," *IEICE Electron. Express*, 14(18), 2017, 20170784.
- [20]. K. P. Rodbell, M. S. Gordon, K. G. Stawiasz, P. Oldiges, K. Lilja, and M. Turowski, "Low energy proton SEUs in 32-nm SOI SRAMs at low V<sub>dd</sub>," *IEEE Trans. Nucl. Sci.*, 64(3), 2017, 999–1005.
- [21]. Z. E. Fleetwood et al., "Using TCAD modeling to compare heavy-ion and laser-induced single event transients in SiGe HBTs," *IEEE Trans. Nucl. Sci.*, 64(1), 2017, 398–405.
- [22]. P. Huang, S. Chen, J. Chen, B. Liang, and R. Song, "The separation measurement of P-hit and N-hit charge sharing with an 'S-Like' inverter chains test structure," *IEEE Trans. Nucl. Sci.*, 64(4), 2017, 1029–1036.