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Design of 4 bit shift register using restructured d flip-flop topology

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ABSTRACT--Low power has emerged as a principal theme in today's electronics industry. To achieve an optimized design, Flip-flops (FF) plays a vital role in low-power digital systems. In the existing method, clock gating with different voltage level signals were implemented such as ,low swing (LS) clock signal and conventional clock, throughout the entire clock network. Thus, power savings was maximized. But, the existing method had a drawback, such as area overhead, had not been quantified. In the proposed method, a restructured DFF is proposed by a pass transistor logic, instead of the inverter setup. A 4 bit serial in parallel out (SIPO) shift register is designed using the restructured DFF and the power and area is reduced by 59%, 12% respectively. The proposed system is implemented using Tanner 13.0 tool with 130 nm technology.

Index Terms – D flip-flop, low swing, restructured D flip-flop, pass transistor.

I.INTRODUCTION

The SIPO shift register proposed in this paper is implemented using the reversible logic gates. The use of the reversible logic gates provide error free output for the given binary input data bits. Therefore, reversible SIPO shift register proposed in this paper provides reduced delay and low power dissipation [1]. The static design is advantaged for longer latching or a slower clock. The dynamic design has better area utilization and yield and can be operated at a higher frequency. Its power consumption is lower, except at high clock frequencies, and the power advantage extends to faster clocks for lower OTFT on/off ratios [2]. The shift register uses a small number of the pulsed clock signals by grouping the latches to several sub shifter registers and using additional temporary storage latches [3]. Modified Clocked Complementary Metal Oxide Semiconductor Latch (mC2MOS Latch) is proposed and delay, power is again reduced up to 60% and the area of the circuit is also reduced [4]. A new method static pass transistor logic (SPTL) is introduced. The SPTL will be reducing the transistor count and power dissipation. The high performance of SPTL is designed and the simulation has been carried out on Tanner EDA Tool [5]. This method solves the timing problem between pulsed latches through the use of multiple non-overlap delayed pulsed clock signals instead of the conventional single pulsed clock signal [6]. Flip flops are the basic storage elements used extensively in all kinds of digital designs. The more transistors there are the more switching and the more power dissipated in the form of heat or radiation. More switching implies higher average current is flowing and therefore the probability of reliability issues occurring rises [7].

In Section II contains the existing method and in Section III proposed method. In section IV contains 4 bit shift register**.** The experimental results are shown in Section V. Finally, concluding remarks are made in Section VI.

II. EXISTING METHOD

In this paper, the Low–voltage/swing technique for lowering the power consumption in clock distribution network. The existing method produces a low swing (LS) clock for low power and high performance applications. Further, that is implemented with a novel D Flip-Flop topology. It enables trustworthy LS operation at the clock sinks while keeping the timing constraints the same. The objective of this method is to lowering the power consumption.

D FLIP- FLOP TOPOLOGY

The DFF topology consisting of nMOS and pMOS transistors, are driven by the clock signals. When the clock signal is high, the pMOS transistors driven by the clock signal fail to completely turn OFF, if the same DFF topology is used with an LS clock signal .To maintain performance, The data ia still at FS. The existing DFF topology as shown in Fig. 1, is simulated with a 130-nm technology node when the clock swing is 0.8 V.

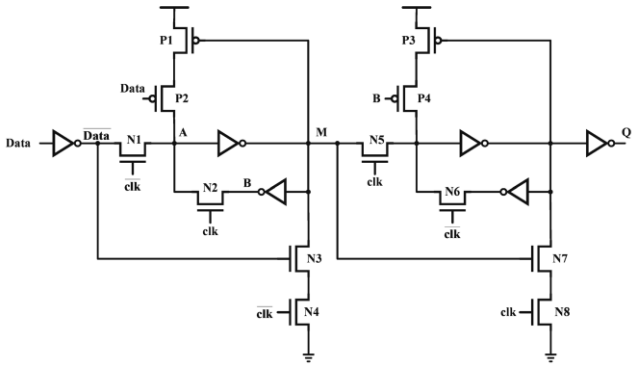


Fig .1. DFF topology

It is mainly used in static DFF. There is nMOS transistor(N1,N2,N5 &N6) are used in both master and slave latches. when LS clock signal is high N1 & N6 can completely turn OFF. It can't transfer full voltage to output voltage, the incoming data signal operate at FS. The following stages the short current and leakage current at node A cannot reach the full load VDD. In addition to increase clock-to-Q delay.A pull-up network consists of two pMOS transistor i.e (p1-p4). It is added to both master & slave latches, when p1 is turn ON the master node N-transistion is low and also data signal is low .p2 and p4 are added to present current when data signal is high and clock signal is low. If N1, is turn on node A become discharge. If p2 does not exist,race condition occur at node A. since N1 is stronger than p1, finaly pull down logic completes this transistion faster.

In this topology, consists of 10 pmos and 14 nmos. As it occupies more area, it is considered as a drawback in existing method.

III PROPOSED METHOD

In the proposed method, D Flip Flop topology is restructured by pass transistor shown in Fig.2, N7 and N5 transistors are removed, an inverter is replaced by a nMOS which act as a pass transistor. When clock is positive the nMOS will conduct and enable the signal. This method have some advantages over existing method. That reduces the parameter,

- Power consumption.
- Area.

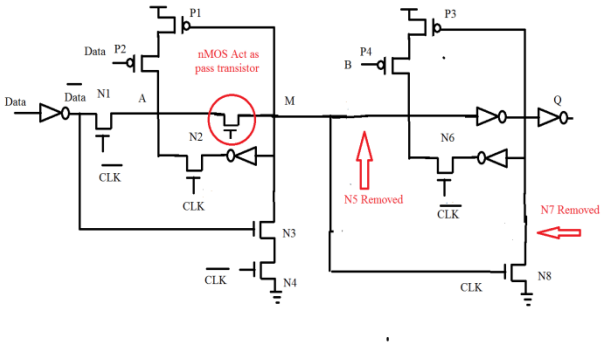


Fig.2.Restructured D Flip-Flop

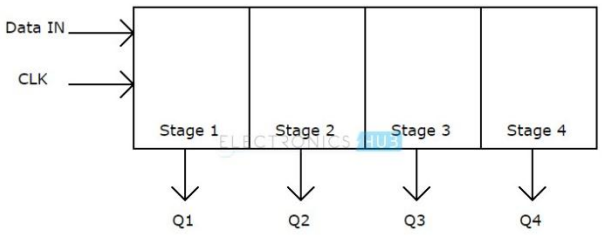
IV 4 BIT SHIFT REGISTERS

In proposed method, A 4 bit shift register of serial in parallel out type is implemented. It also reduces power consumption and area. A number of flip flops are connected in series, this arrangement is called a Register. The stored information can be transferred within the registers; these are called as 'Shift Registers'. A shift register is a sequential circuit which stores the data and shifts it towards the output on every clock cycle.
Basically shift registers are of 4 types. They are

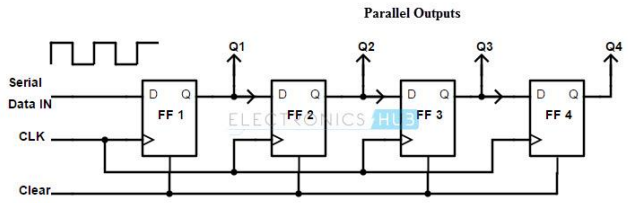
- Serial In Serial Out shift register
- Serial In parallel Out shift register
- Parallel In Serial Out shift register
- Parallel In parallel Out shift register

SERIAL IN PARALLEL OUT SHIFT REGISTER

The input to this register is given in serial and the output is collected in parallel.



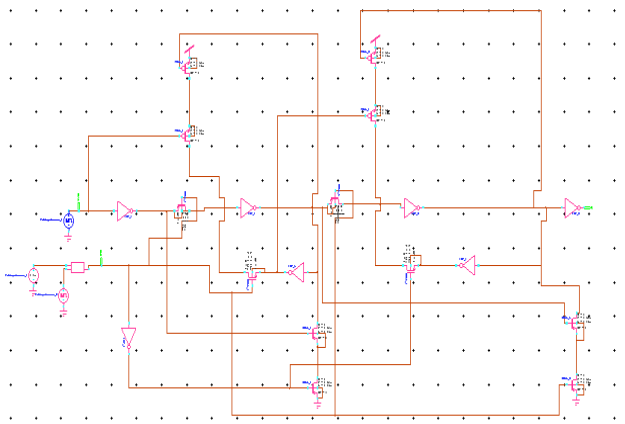
The clear (CLR) signal is connected in addition to clock signal to all the 4 flip flops in order to RESET them and the serial data is connected to the flip flop at either end (depending on shift left register or shift right register). The output of the first flip flop is connected to the input of the next flip flop and so on. All the flip flops are connected with a common clock.



Unlike the serial in serial out shift registers, the output of Serial in Parallel out (SIPO) shift register is collected at each flip flop. Q1, Q2, Q3 and Q4 are the outputs of first, second, third and fourth flip flops, respectively. The main application of Serial in Parallel out shift register is to convert serial data into parallel data. Hence they are used in communication lines where demultiplexing of a data line into several parallel line is required.

V.EXPERIMENTAL RESULTS

The Existing method describes that the LSDFF cell is designed by using tanner EDA 13.0 tool with 130 nm technology. The DFF cell successfully latches both logic-low and logic-high FS data signals after the rising edge of the LS clock signal. The output signal reaches nominal (FS) VDD, and the DFF cell does not exhibit glitches in any of the internal nodes. DFF topology that can reliably work with an LS clock signal whereas the data and output signals are at FS shown in Fig.3(a). And the output performance has shown in fig 3(b).



Fg .3(a) LS clock signal whereas the data and output signals are at FS, (a) transistor level representation

By using the 130nm technology it easily glitches the level of power supply from 5v to 3v.Due to this the power consumption may reduces to 0.3v. Its the highest power consumption. Apart from this the working process of the circuit may not disturbed and glitches may not occur. The output representation of Existing method is identified in Fig 3(b).

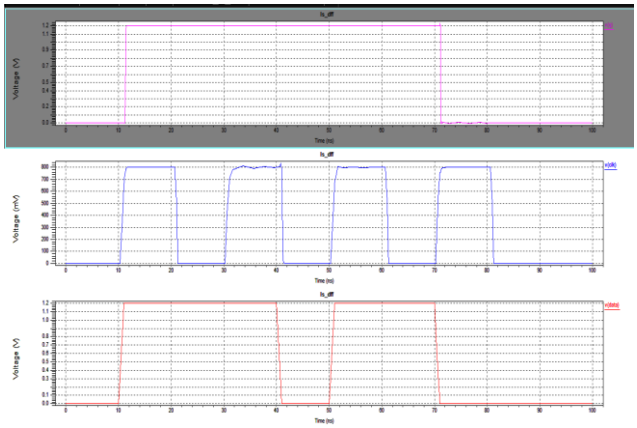


Fig .3 (b) output performance

The proposed restructured DFF is modified from existing method and simulated circuit as shown in fig 4(a) and the data and output signals are same logic at shown fig 4(b). Thus, power consumptions and area reduced.

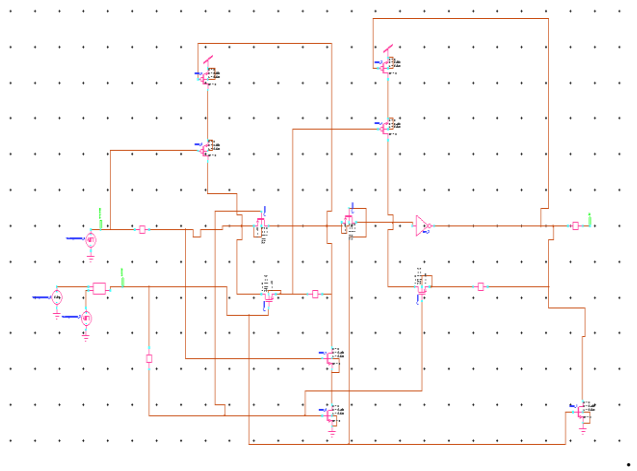


Fig. 4(a) restructured DFF schematic level representation.

This simulation also carried by tanner 130 nm technology and simulation results shows that, the power and area is diminished up to 59%, 12% respectively.

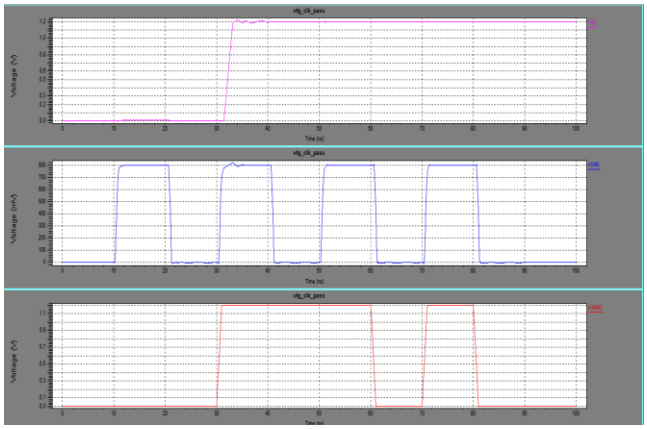


Fig.4(b) simulation output

A 4 Bit shift register implemented using both existing method D Flip-Flop and Restructured D Flip-Flop shown in Fig.5(a). There are serial in parallel out type of shift register presented. Each flip flop contains inputs and single output from previous Flip-Flops.

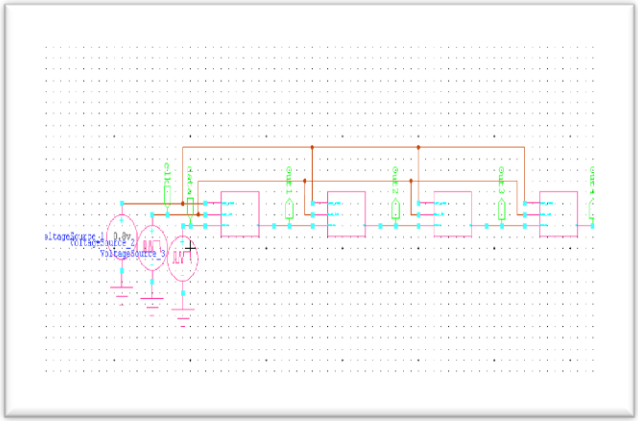


Fig. 5(a) 4 Bit shift register implemented by restructured DFF

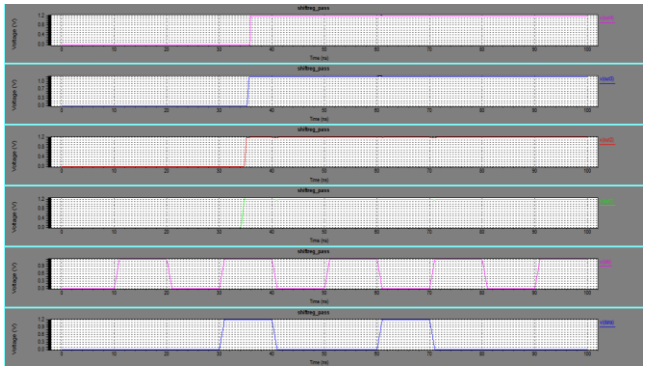


Fig.5.(b) 4Bit Shift registers Using Restructured DFF Output Waveform

Table 1: Comparision of 4 bit shift registers using DFF and restructured DFF.

Parameter Analyzed	No. of PMOS	No. of NMOS	Power consumption (m W)	Delay (ns)	Power-Delay Product (Joules)
4 Bit shift register using DFF method	40	56	0.084	0.168	0.0141
4 Bit shift register using restructured DFF Method	36	48	0.034	0.168	0.0057

V.CONCLUSION

In the proposed method, A 4 bit serial in parallel out shift register is implemented using the reconstructed DFF. In this method the area and power is reduced by eliminating the needless transistors and inverters using pass transistors. The experimental results shows on Table 1, the power and area is diminished up to 59%, 12% respectively. The delay is also remains same as compared with the existing method. An optimized shift register is designed with minimum power consumption and area as compared with the presented method.

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