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A review on VLSI design techniques for power optimization

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Abstract—**This review paper gives the introduction of the various VLSI Design techniques. Low power has emerged as an important factor in today's world of electronics industries. The reduction of logic circuit power consumption is a major priority of a designer attempting to meet implementation requirements. Power dissipation is a matter of concern as far as designing high performance systems are concerned. This makes clock signals a great source of power dissipation. High frequency systems use a large number of clock pulses. Whereas clock signals are only used for synchronization of the circuits the power dissipation due to clock pulses is significant making it important to study and area is one of the main objectives in all VLSI circuits. Power optimization is the use of electronic design automation tools to optimize (reduce) the power consumption of a digital design.**

Index Terms— **Low power, Power Dissipation, Power Optimization**

I. INTRODUCTION

Now a day's power is the primary concerned due to the remarkable growth and success in the field of personal computing devices and wireless communication system which demand high speed computation and complex functionality with low power consumption. The main reason behind popularizing low power is new generation of portable devices which includes laptops, palm tops, mobile phones etc. Thus apart from performing at high speeds the devices must also work at low power to satisfy human needs. Thus it has become imperative to consider power consumption as a very important and significant design concern. Scaling of technology node increases power-density more than expected. Proportion of digital circuits is designed to be synchronous circuits. The most popular synchronous digital circuits are edge triggered flip flops. The total clock related power consumption in synchronous VLSI circuits is due to power consumption in the clock network, power consumption in the clock buffers, and power consumption in the flip-flops. The basic techniques for low power design are clock gating for reducing dynamic power, multiple threshold voltage to decrease leakage current. In CMOS technology, the power dissipation is mainly contributed by static and dynamic power. The main

components that affect power dissipation are capacitive load currents, short circuit currents and leakage currents. Static power dissipation occurs due to leakage currents and sub threshold currents that contribute a small percentage to the total power consumption. Five main sources of leakage currents in CMOS transistors are sub threshold leakage (ISUB), gate oxide tunneling leakage (IG), reverse-bias source/drain junction leakages (IREV), gate induced drain leakage (IGIDL) and gate current due to hot-carrier injection (IH)

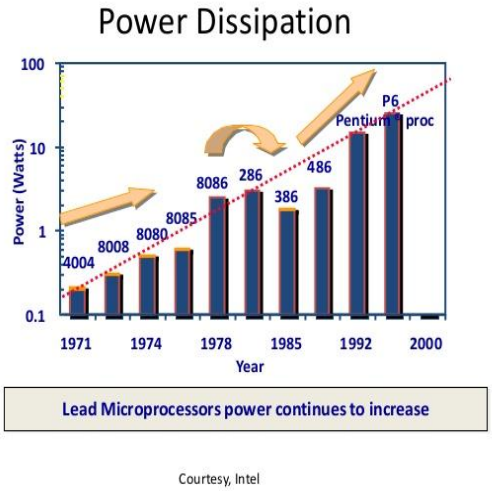

Figure 1. Evolution in Power dissipation

2. STRATEGIES FOR LOW POWER DESIGNS.

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There are different strategies in VLSI design process for reducing the power consumption. The strategy used for 1) operating system level is portioning and power down, 2) Software level is Regularity, locality and concurrency, 3) Architecture level is Pipelining, Redundancy and data encoding 4) Circuit/Logic level is logic styles, transistor sizing and energy recovery 5) Technology level is threshold reduction, multi threshold devices. Effective power consumption is possible by using the different strategies at various levels in VLSI design process. So, designers need a particular approach for optimizing power consumptions in designs.

3. POWER DISSIPATION

CMOS logic dissipates less power than NMOS logic circuits because CMOS dissipates power only when switching ('dynamic power'). NMOS logic dissipates power whenever the output is low ('static power'), because there is a current path from Vdd to Vss through the load resistor and the n-type network. Static CMOS gates are very power efficient because they dissipate early zero power when idle.

Static dissipation is due to **a) Sub threshold condition:** when the transistors are off both NMOS and PMOS transistor has a gate source threshold voltage, below which the current through the device drops exponentially.**b) Tunneling:** Current through Gate Oxide Sio2 is a very good insulator, but at very small thickens levels electrons can tunnel across the very thin insulation the probability drops off exponentially with oxide thickness. **c) Leakage Current** through reverse bias diodes. These are small reverse leakage current which is formed due to formation of reverse biased between diffusion regions and wells.

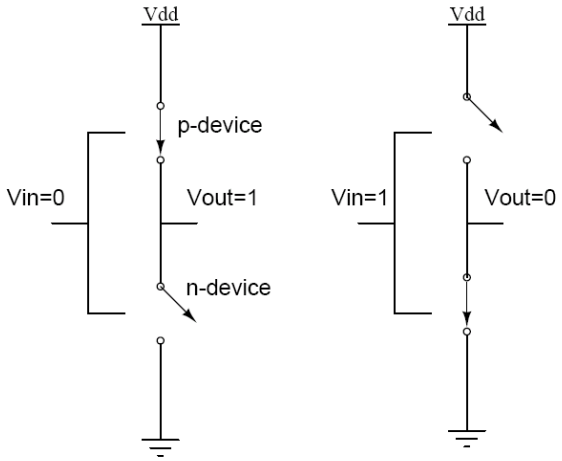

Figure 2. Static power dissipation

Dynamic power dissipation is due to charging and discharging of load capacitances .In one complete cycle of CMOS logic, current flow from V_{dd} to the load capacitance to charge it and then flows from the charged load capacitance to GND during discharge. Therefore in one complete charge/discharge cycle, a total $Q= C_L V_{DD}$ is thus transferred from V_{DD} to ground. Multiply by the switching frequency on the load capacitances to get the current used, and multiply by voltage again to get the characteristic switching power dissipated by a CMOs device.

Since most gates do not operates/switch at every clock cycle they are often accompanied by a factor α, called the activity factor.

$$P_{dynamic} = \alpha C V^2_{DD} f$$

The power dissipated can be reduced by reducing either the clock frequency, or the load capacitance, or the rail voltage, or the switching activity parameter, α. Reducing the clock frequency is the easiest thing to do, but it seriously affects the performance of the chip. Applications where power is paramount, this is approach can be used satisfactorily. Another method to reduce the dissipated power is to lower the load capacitance. But this method is more difficult than the previous approach because it involves conscientious system design, so that there are fewer wires, smaller pins, smaller fan-out, smaller devices etc. Power dissipation can also be reduced by reducing the rail voltage. But this can be done only through device technology. Also rail voltage is a standard agreed to in many cases by the semiconductor industry, hence we do not have much control over this parameter. Also rail voltage is strongly dependent on the threshold voltage and the noise margin. Some special techniques are also used to reduce power dissipation. The first one involves the use of pipelining to operate the internal logic at a lower clock than the i/o frequency. The other technique is to reduce switching activity, α, by optimizing algorithms, architecture, logic topology and using special encoding techniques.

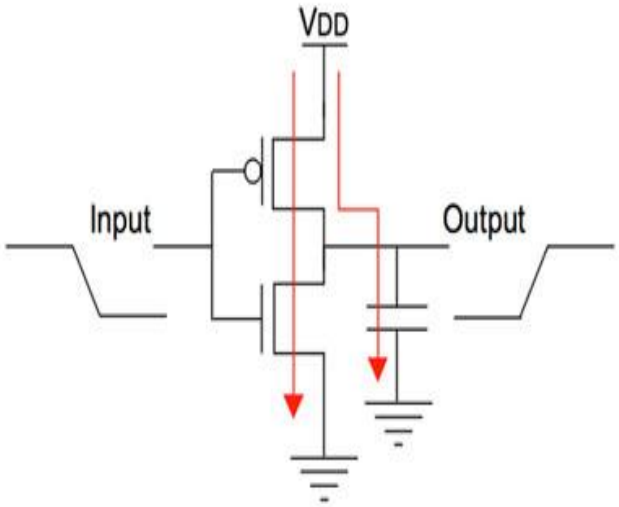

Figure 3.Dynamic Power Dissipation

Short Circuit power Dissipation ,there is a finite Rise/fall time for both PMOS and NMOS, during transition, say from OFF to ON, both the transistors will be ON for a small period of time in which Current will find a path directly from V_{DD} to

GND. Short circuit power dissipation increases with rise and fall time of the transistors.

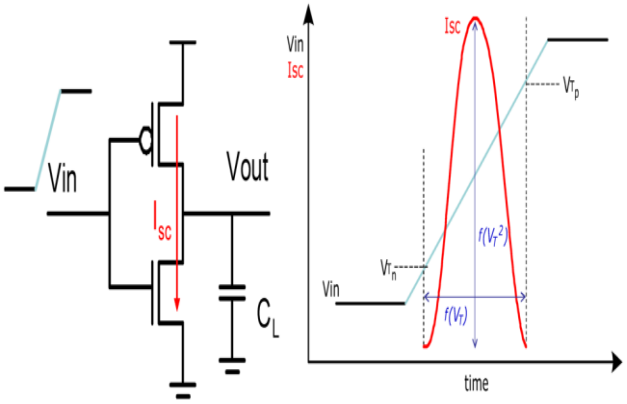

Figure 4. Short Circuit Power Dissipation

4. LOW POWER DESIGN PRINCIPLES

Dynamic power dissipation is greater than static power dissipation when systems are active. For high performance systems such as workstations and servers, dynamic power consumption per chip limited to 150 W.

4.1 Dynamic Power Reduction

Dynamic power can be reduced by decreasing the following factors.

Activity Factor: Static logic has a low activity factor. Clocked nodes have an activity factor of 1. Clock gating can be used to stop portions of the chip that are idle. Turn off the clock network wherever possible. Sense the chip temperature and cut back activity, if the temperature becomes too high.
Switching Capacitance: This is reduced by choosing small transistors. Small gates can be used on non-critical paths. Buffer driving I/O pads and long wires use a stage effort of range 8-12 to reduce the buffer size.
Power Supply: Choosing low power supply reduces power consumption. Voltage can be adjusted on operating mode.
Operating Frequency: In a digital signal processing system, two multipliers running at half speed can be replaced by a single multiplier at full speed to reduce power consumption.

4.2 Static Power Reduction

This involves minimizing I_{static} Analog current sources and pseudo-nMOS gates are turned off when they are not needed. Sub threshold leakage can be controlled through the body voltage using the body effect. Reverse Body Bias can be used during the idle mode to reduce leakage. Forward Body Bias can be used during the active mode to increase the performance. Another method to reduce idle leakage current is to turn off the power supply entirely. This is done externally with the voltage regulator or internally with a series transistor.

5. LOW POWER DESIGN TECHNIQUES

There are different techniques available for low power design.

Clock Gating is a popular technique used in many synchronous circuits for reducing dynamic power dissipation. Clock gating saves power by adding more logic to a circuit to prune the clock tree. Pruning the clock disables portions of the circuitry so that the flip-flops in them do not have to switch states. Switching states consumes power. When not being switched power consumption goes to zero, and only leakage currents are incurred.

Power Gating is a technique used in integrated circuit design to reduce power consumption, by shutting off the current to blocks of the circuit that are not in use. In addition to reducing stand-by or leakage power, power gating has the benefit of enabling Iddq testing.

Variable Frequency: In a big chip, not all the blocks need to be clocked at highest possible frequency in order to achieve the desired level of performance. There can be few blocks which inherently work slow and therefore, can be clocked at slower clock than blocks like core which required high frequency clock for maximum throughput. Therefore, by providing different frequency clocks to different blocks, one can reduce localized dynamic consumption.

Multi Threshold Voltage CMOS Cells: A lot of MOS characteristics are governed by the threshold voltage of the cell. Sub-threshold current is the current between source and drain when the gate voltage is below threshold voltage.

Multi Vdd Technique: There is a quadratic relationship between device voltage Vdd and dynamic power consumption. Therefore one can reduce the dynamic voltage substantially by reducing the supply voltage.

Traditional Techniques	Dynamic power reduction	Leakage power reduction	Other power reduction techniques
--Clock gating	--Clock gating	--Minimize usage of low Vt cells	--Multi oxide devices
--Power gating	--Power efficient circuits	--Power gating	--Minimize capacitance by custom design
--Variable frequency	--Variable frequency	--Back biasing	--Power efficient circuits
--Variable voltage supply	--Variable voltage supply	--Reduce oxide thickness	
--Variable device threshold	--Voltage Islands	--Use FinFET	

Fig.5. Low power Design techniques

6. POWER OPTIMIZATION TECHNIQUES.

Power optimization is the use of electronic design automation tools to optimize (reduce) the power consumption of a digital design, such as that of an integrated circuit, while preserving the functionality. Many different techniques are used to reduce power consumption at the circuit level. Some of the main ones are:

Transistor sizing: adjusting the size of each gate or transistor for minimum power.

Voltage scaling: lower supply voltages use less power, but go slower.

Voltage islands: Different blocks can be run at different voltages, saving power. This design practice may require the use of level-shifters when two blocks with different supply voltages communicate with each other.

Variable V_{DD}: The voltage for a single block can be varied during operation - high voltage (and high power) when the block needs to go fast, low voltage when slow operation is acceptable.

Multiple threshold voltages: Modern processes can build transistors with different thresholds. Power can be saved by using a mixture of CMOS transistors with two or more different threshold voltages. In the simplest form there are two different thresholds available, common called High-Vt and Low-Vt, where Vt stands for threshold voltage. High threshold transistors are slower but leak less, and can be used in non-critical circuits.

Power gating: This technique uses high Vt *sleep transistors* which cut-off a circuit block when the block is not switching. The sleep transistor sizing is an important design parameter. This technique, also known as MTCMOS, or Multi-Threshold CMOS reduces stand-by or leakage power, and also enables Iddq testing.

Long-Channel transistors: Transistors of more than minimum length leak less, but are bigger and slower.

Stacking and parking states: Logic gates may leak differently during logically equivalent input states (say 10 on a NAND gate, as opposed to 01). State machines may have less leakage in certain states.

Logic styles: dynamic and static logic, for example, have different speed/power tradeoffs.

7. CONCLUSION

In this paper, various strategies and techniques for reduction in power has been discussed. This paper has successfully reviewed the CAD methods for power optimization keeping pace with area, delay and performance. This works elaborated the need for low power VLSI circuits and suggested various design techniques currently in practice in microelectronics industry. This paper will help the designers to understand the basics of low power.

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